(Extremely efficient) clocked electron transport on superfluid helium

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Extremely efficient clocked electron transport on superfluid helium

Outline

1. Intro
   What can we do with mobile electrons?
2. Sandia Device
   Clocking experiment
3. IBM Device
   What’s next?
Electrons on superfluid helium

Clean system: Electrons in vacuum

Long spin coherence
negligible spin-orbit interaction

⇒ Able to move electrons without spin decoherence!
Transport enabled computation

Memory registers

Interaction

Dot

Single charge
Transport enabled computation

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Single charge
Channel Device with Sandia CMOS7
Channel Device with Sandia CMOS7
Experiment
Sandia Device

120 parallel channels

Wide Reservoir

Narrow Reservoir

Right and Left Memory Cell Gates

Vertical CCD

Measurement Gates

Wide Reservoir

Narrow Reservoir

2 mm

6 mm

2um He

3um

SiO₂
3-phase CCD
Potential

Underlying gates

Helium

Potential Energy

electron
Potential Energy

3-phase CCD

Clocking 8
Electron has moved one pixel (3 gates) to the right
Measurement

Modulate twiddle to push electron on and off the sense gate

HEMT Preamp at 1.5 K
Horizontal CCD

Loading:
- Photoemit electrons on plates
- Load them to pixels by opening the door

Clocking Sequence
- 10 pixel to the left
- 10 pixel back to the right
Horizontal Clocking Efficiency

Clock (pixel) rate = 240kHz

No measurable errors

pixels transferred

~ 70 min.

~ 9 km.
Vertical Clocking
Vertical Clocking
Vertical Clocking
Vertical Clocking
Vertical Clocking
Vertical Clocking

Sense
Channel Occupancy

![Graph showing channel occupancy with initial signal of approximately 13.5 electrons per channel.](image)
Vertical Clocking
Vertical Clocking
Vertical Clocking

60 Channels

60 Channels
Vertical Clocking

60 Channels

60 Channels
Vertical ("C-cycle") Efficiency

Vertical ("C-cycle") Efficiency

Channel occupancy after C-Cycle

High Density Loading
Medium Density Loading
Conclusions for electrons on superfluid helium channels with silicon integrated circuits (Sandia device)

- Unprecedented reliability of a Charge Coupled Device
  - Essentially a perfect Electron Transfer Efficiency

- 5 clock lines for full control
  - 2D Scalability: Move anywhere in our ~5000 position gate & channel array

- Si-Processing
  - First, non-optimized design with standard silicon processing
  - Possibilities for on-chip amplification
  - On-chip multiplexer
  - More...

Bradbury, Takita et al. PRL 107, 266803 (2011)
IBM CMOS

8 metal layers (Aluminum and Copper)

Silicon

SiO₂

Etch
IBM CMOS

Channels using thin metals

Top Ground

Gates

SiO$_2$

M1

M5

Silicon
IBM CMOS

2mm
IBM CMOS

Filling and cheesing!!!!

Electroplating? Electro chemistry?
IBM CMOS

Turnstile
Single Electron loading

ONE AT A TIME!!!
IBM CMOS

- Turnstile
- Quantum dots

Need better sensing
On-chip amplification?
What else?
IBM CMOS

- Turnstile
- Quantum dots

Twiddle Sensor: Potential Simulations

Top metal plane held at -3V

Twiddling right:

<table>
<thead>
<tr>
<th>Φ3</th>
<th>Twiddle</th>
<th>Sense</th>
<th>Door</th>
<th>Plate1</th>
</tr>
</thead>
<tbody>
<tr>
<td>-400mV</td>
<td>-80mV</td>
<td>0mV</td>
<td>-320mV</td>
<td>-400mV</td>
</tr>
</tbody>
</table>

Twiddling left:

<table>
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<tr>
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<th>Twiddle</th>
<th>Sense</th>
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</tr>
</thead>
<tbody>
<tr>
<td>-400mV</td>
<td>+80mV</td>
<td>0mV</td>
<td>-480mV</td>
<td>-400mV</td>
</tr>
</tbody>
</table>

3 um channels
2.5 um wide gates

Electrical potential in volts at the helium surface above the channels

Need better sensing
On-chip amplification?
What else?
Wider gates!!!

- 6 X 6 um Sense gate
- Gate in between Sense and Twiddle
What do we do for our next chip???

1. Narrower channels (avoid filling)
2. Narrower gates (avoid cheesing)
3. Some wider gates (better sensing)
4. Turnstile
5. Quantum dots
6. On-chip amplifiers

THANK YOU