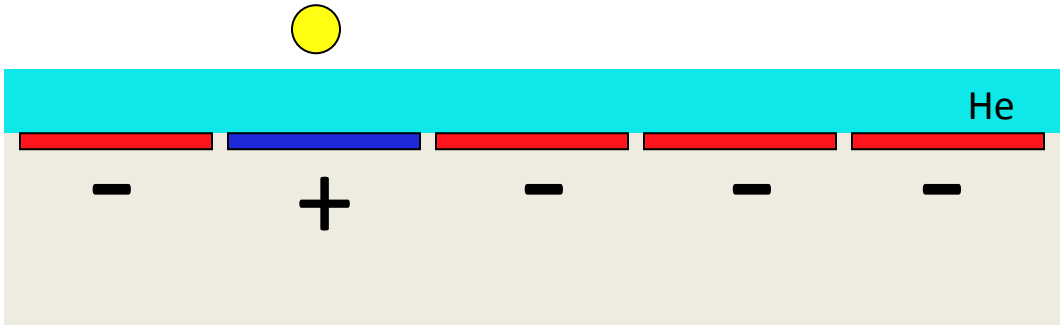
(Extremely efficient) clocked electron transport on superfluid helium



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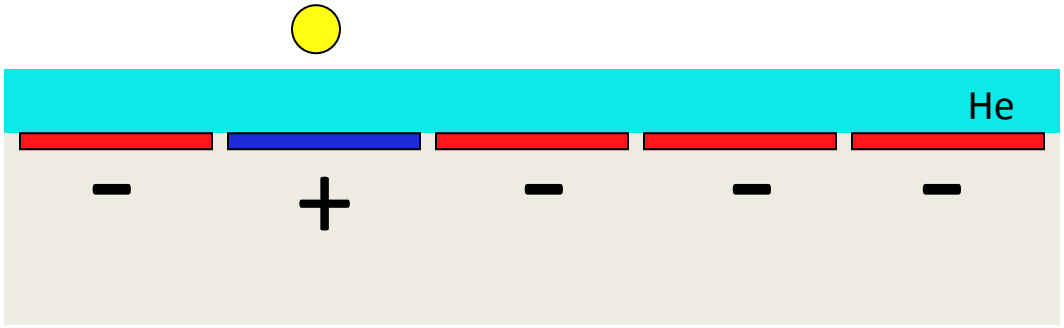
2. Present address: HRL Laboratories, LLC, Malibu, CA, USA

Extremely efficient clocked electron transport on superfluid helium



Outline

1. Intro

   What can we do with mobile electrons?

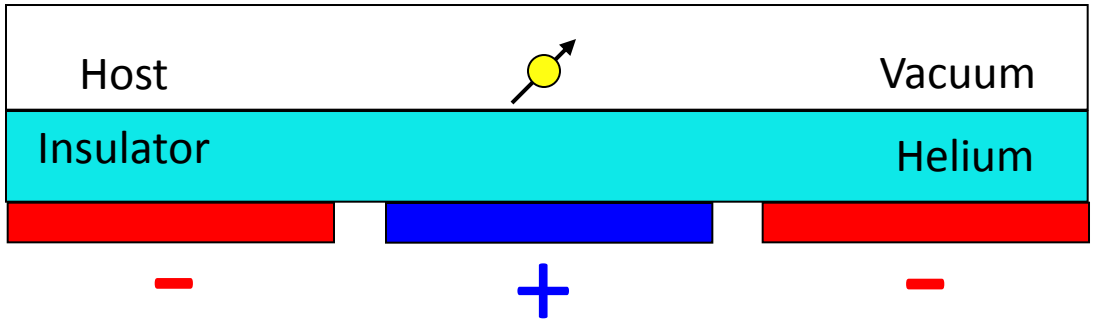
2. Sandia Device

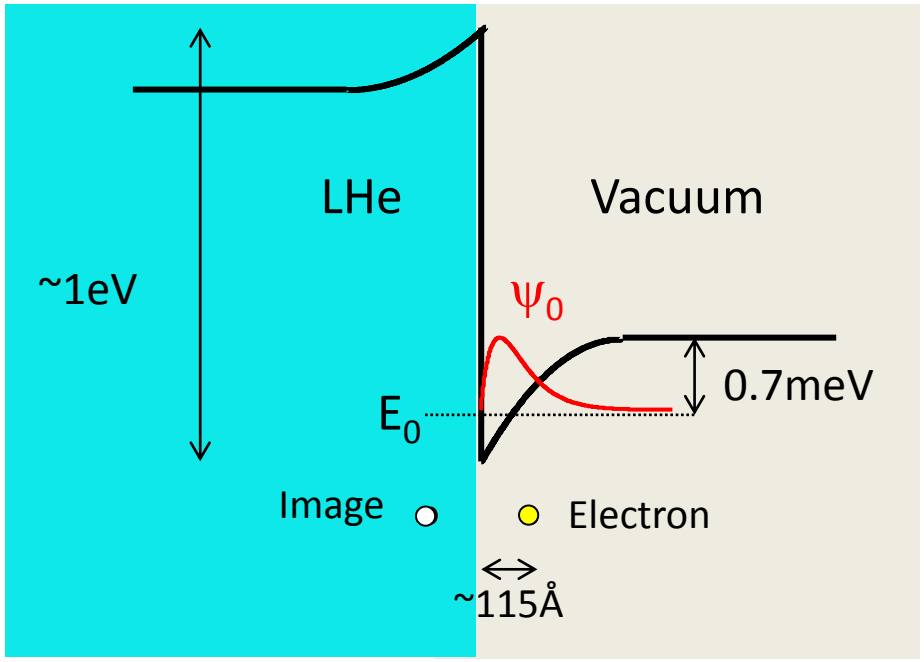
   Clocking experiment

3. IBM Device

   What's next?

Electrons on superfluid helium





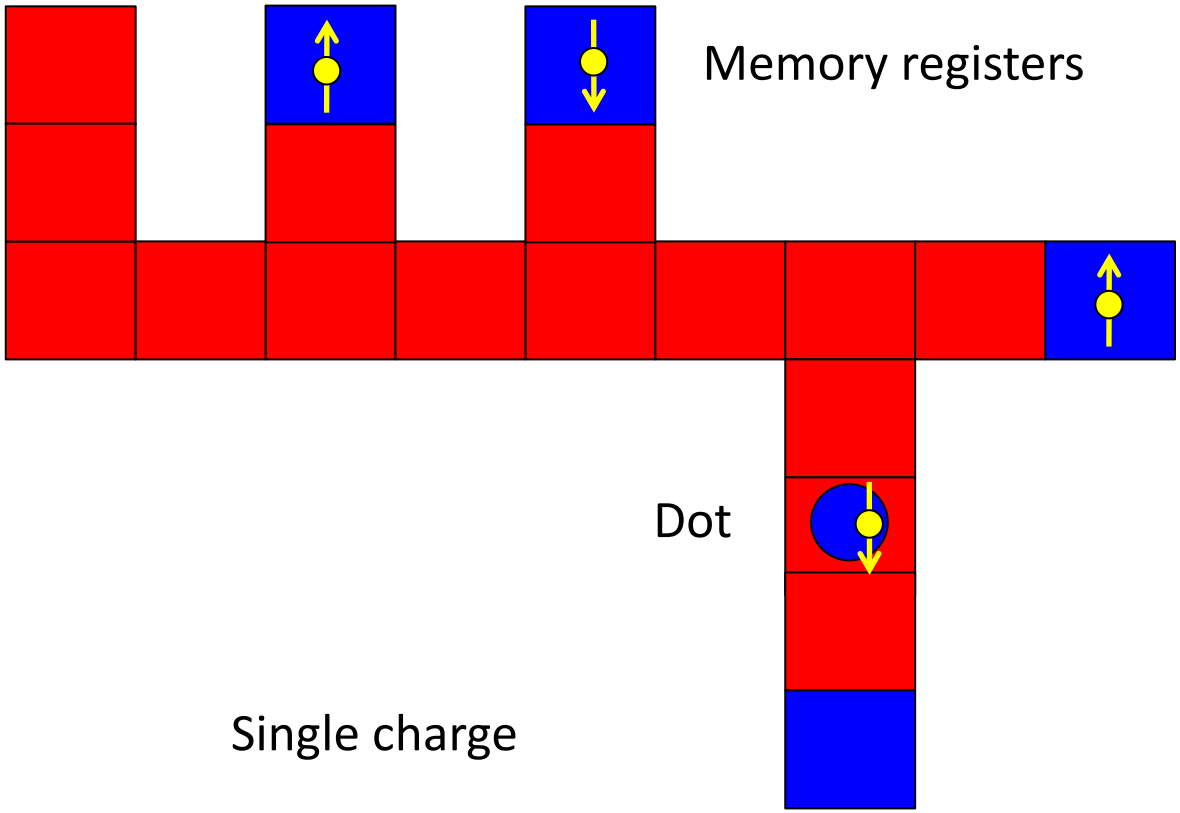
Clean system: Electrons in vacuum

Long spin coherence

negligible spin-orbit interaction

$\Rightarrow$ Able to move electrons without spin decoherence!

Transport enabled computation



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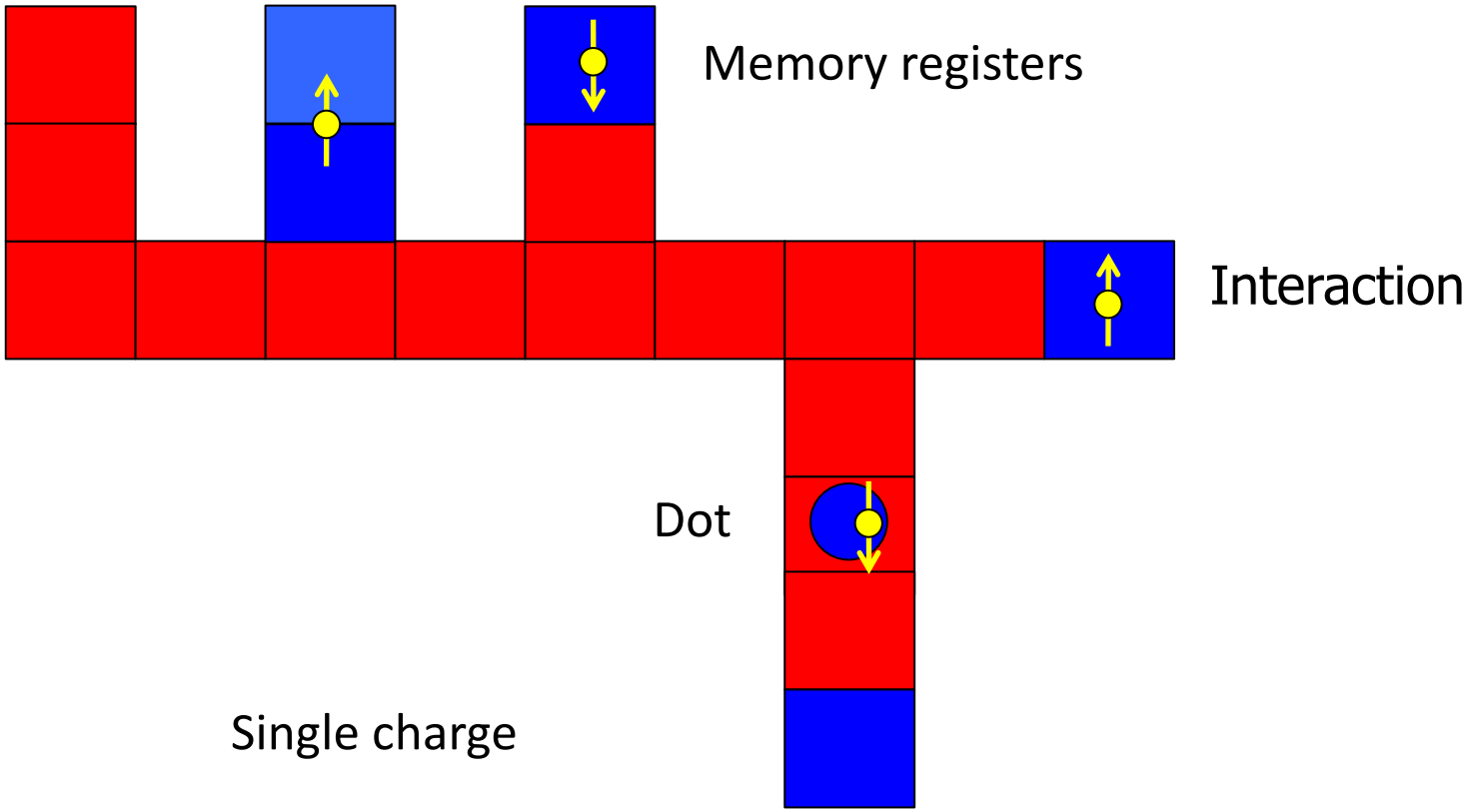

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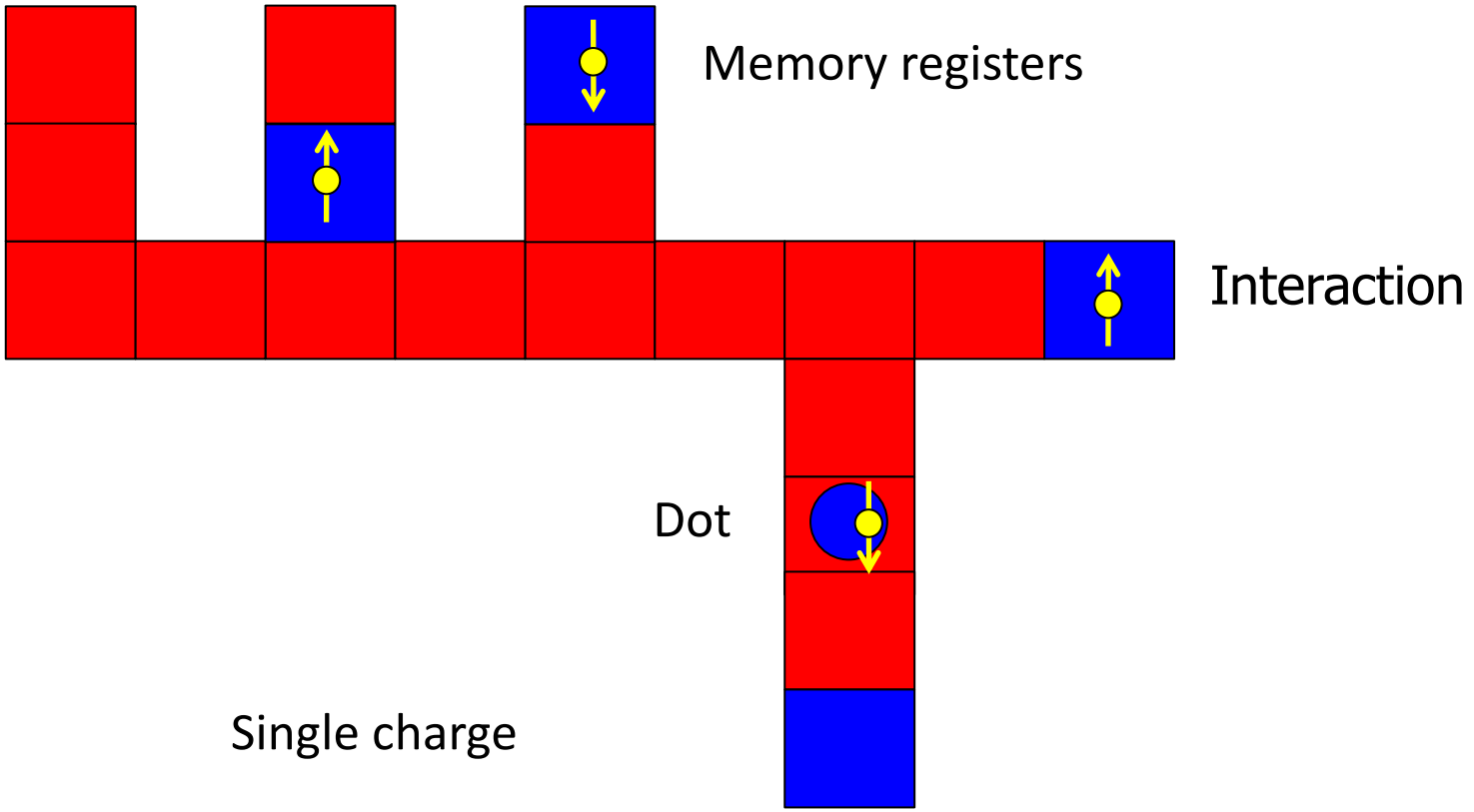

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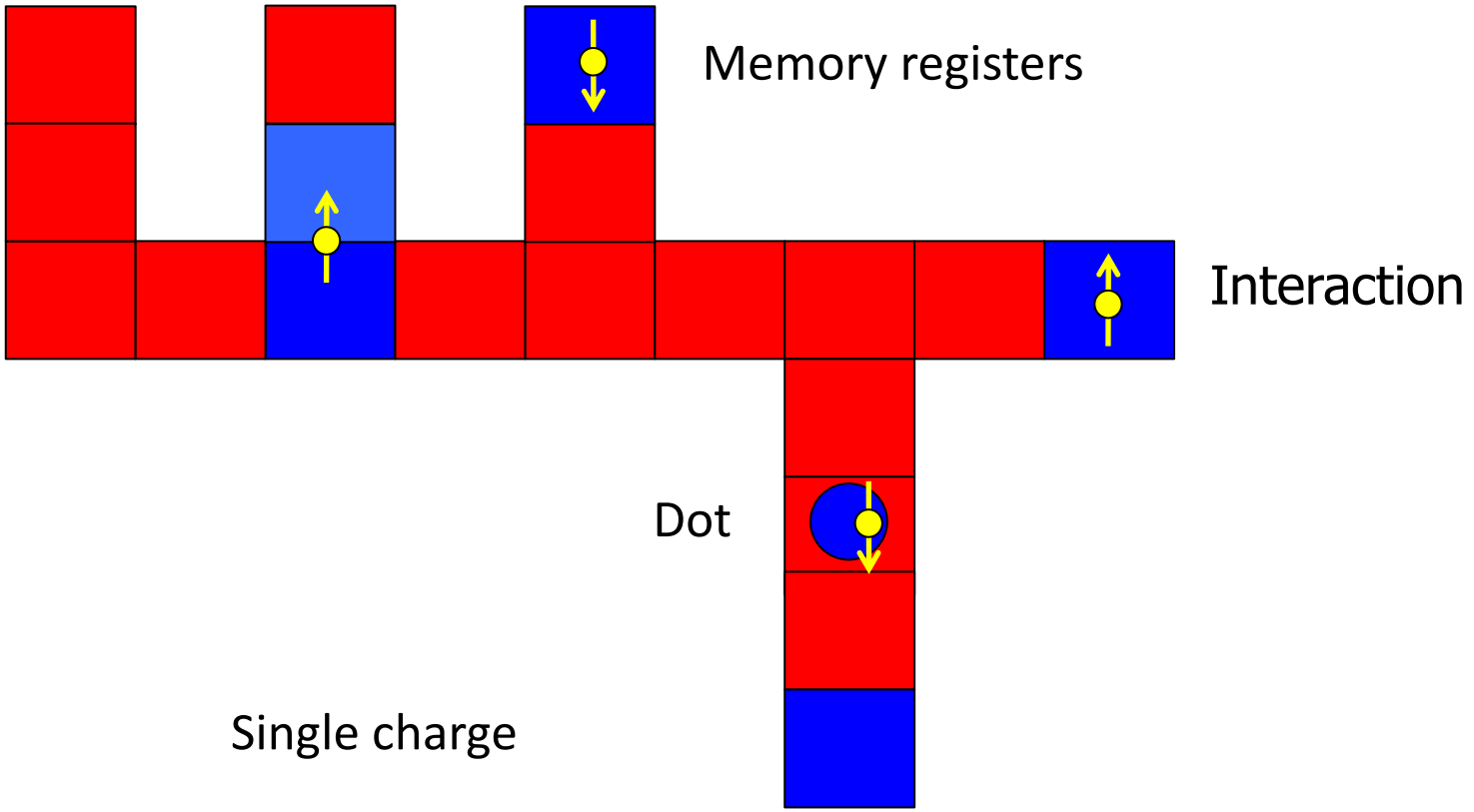

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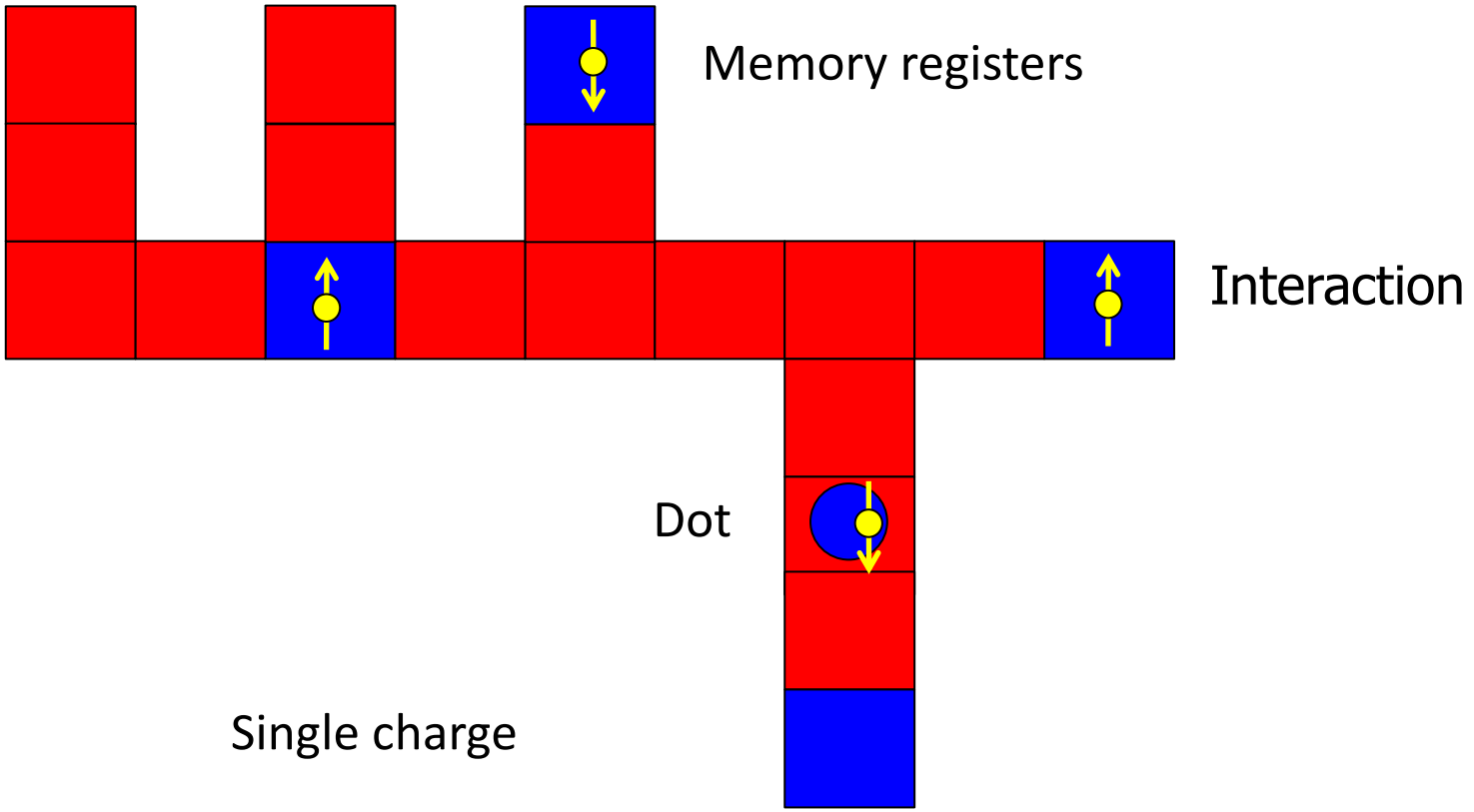

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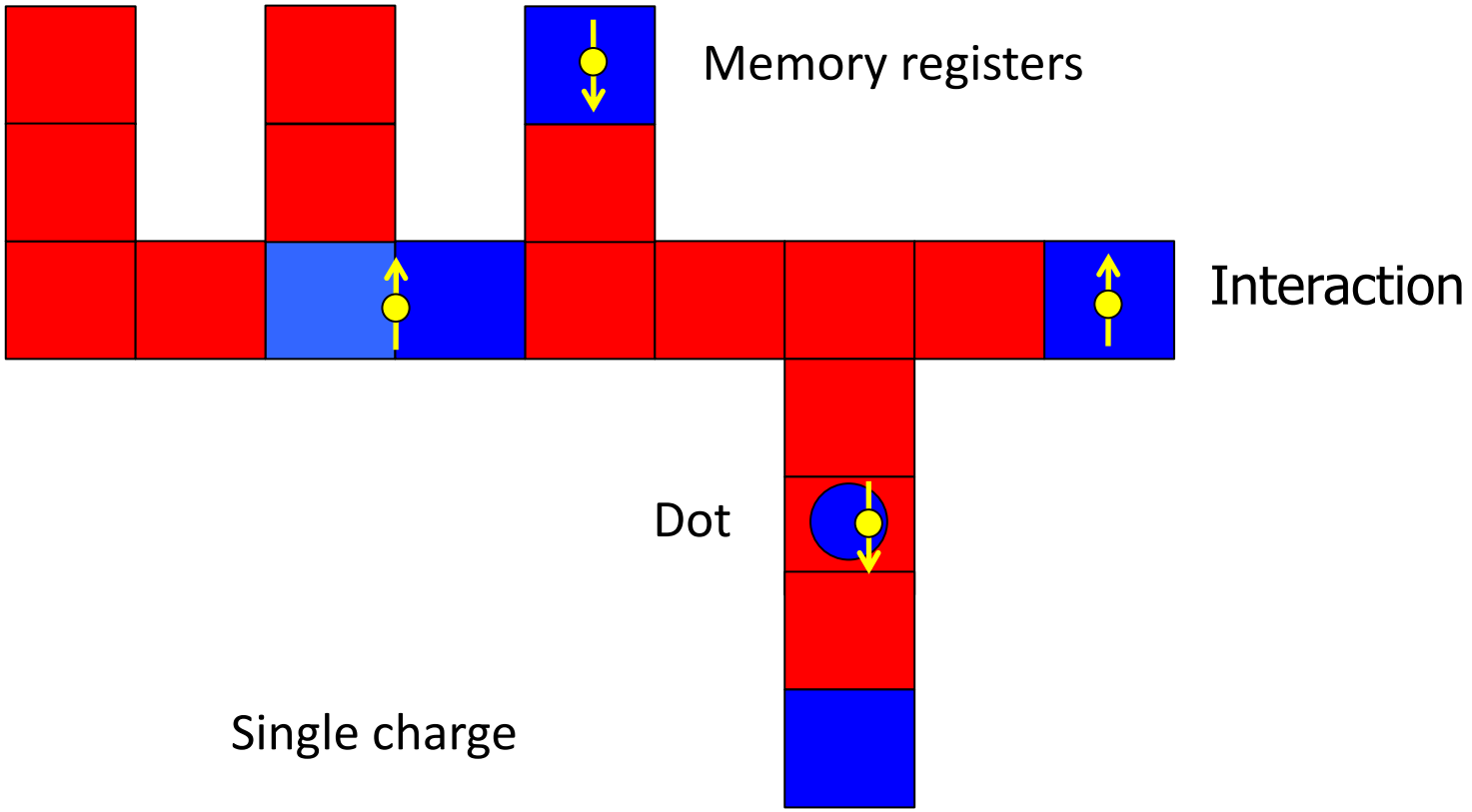

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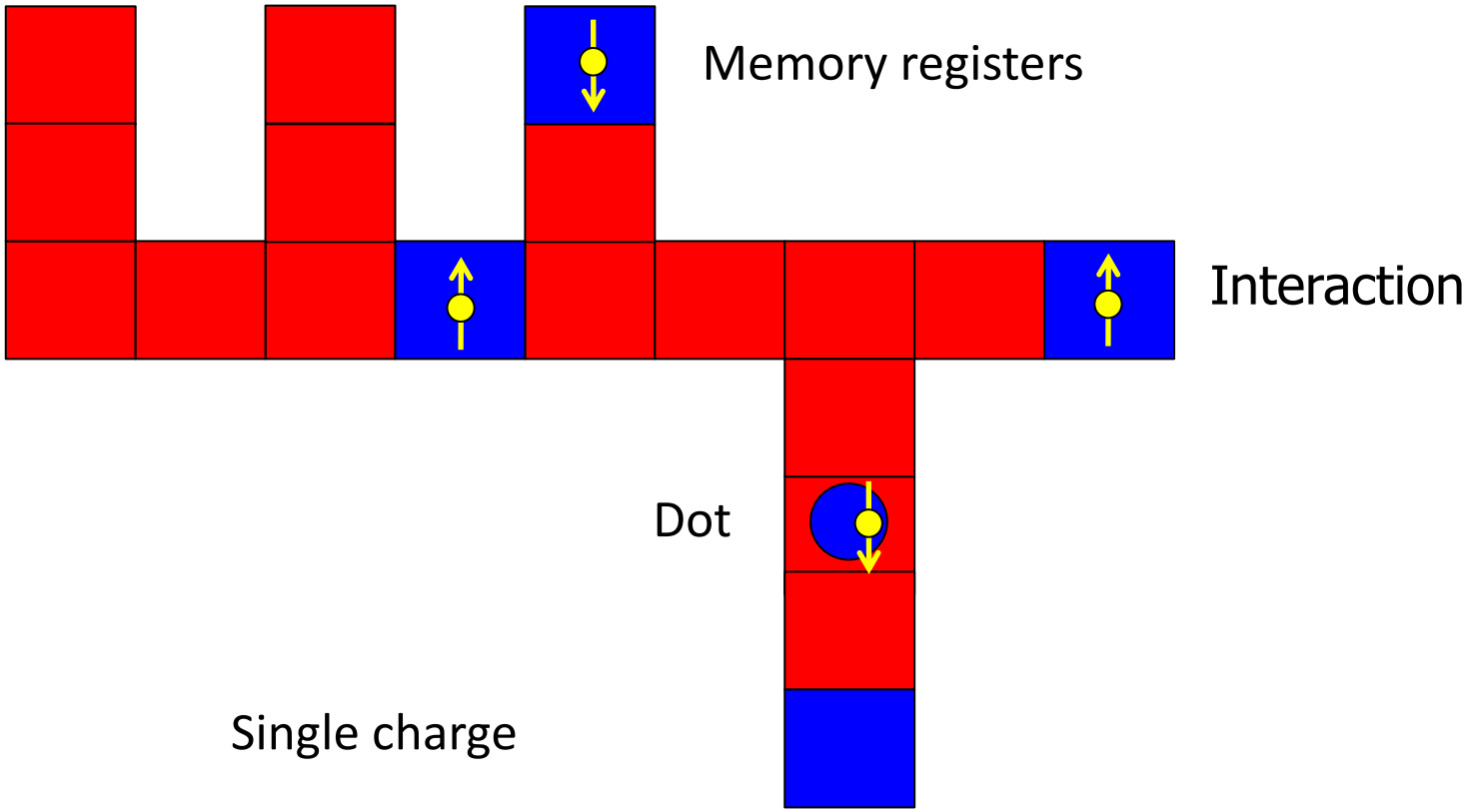

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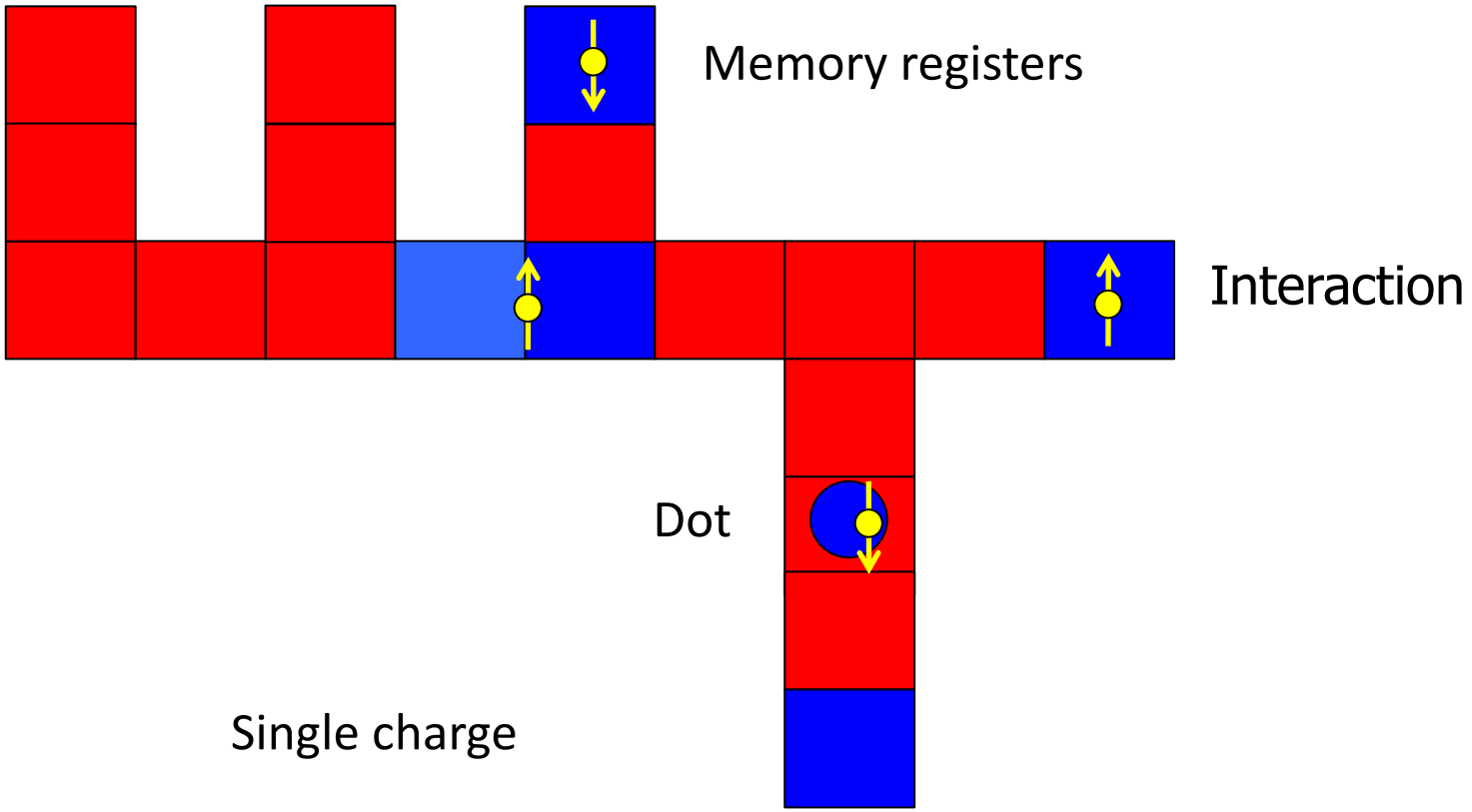

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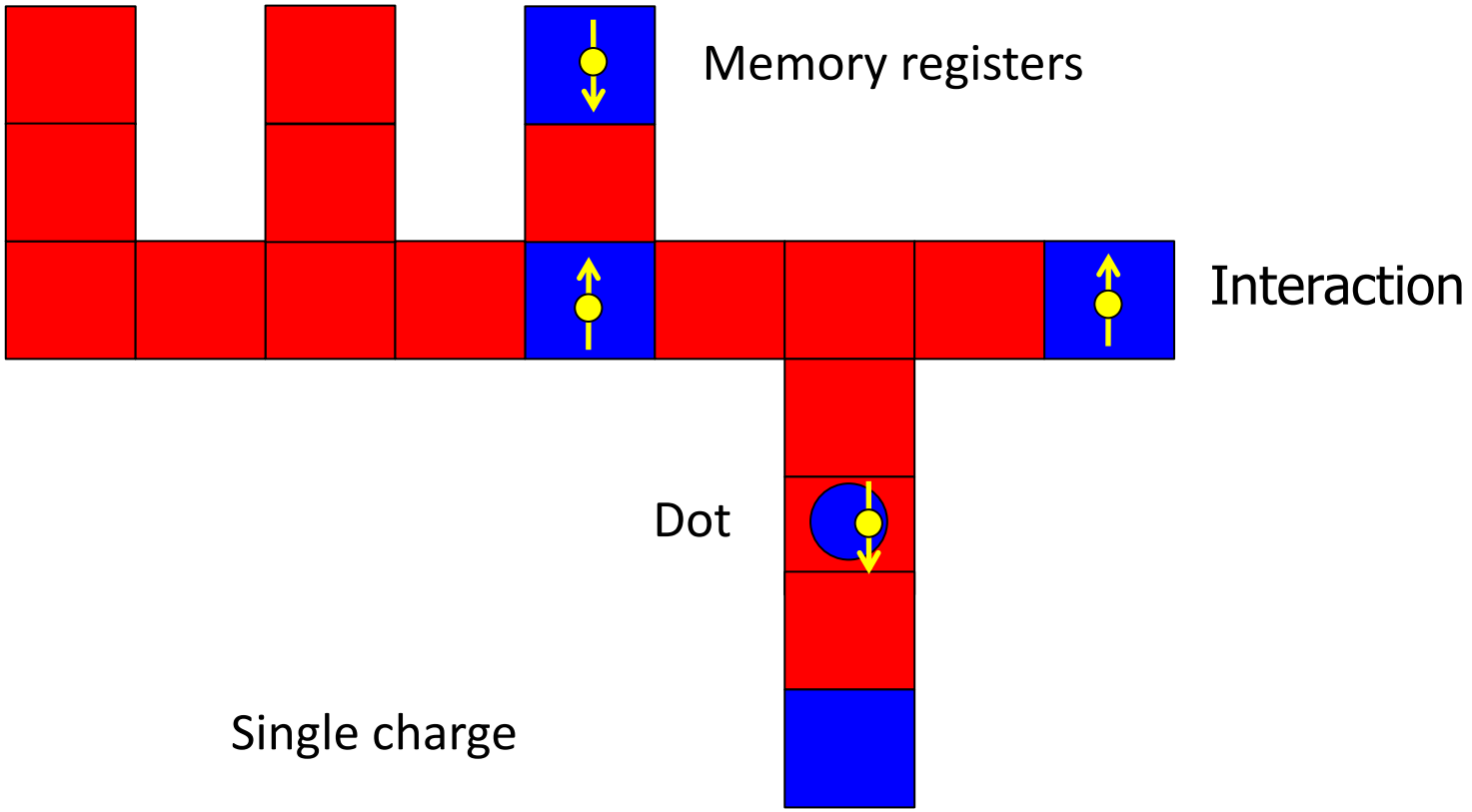

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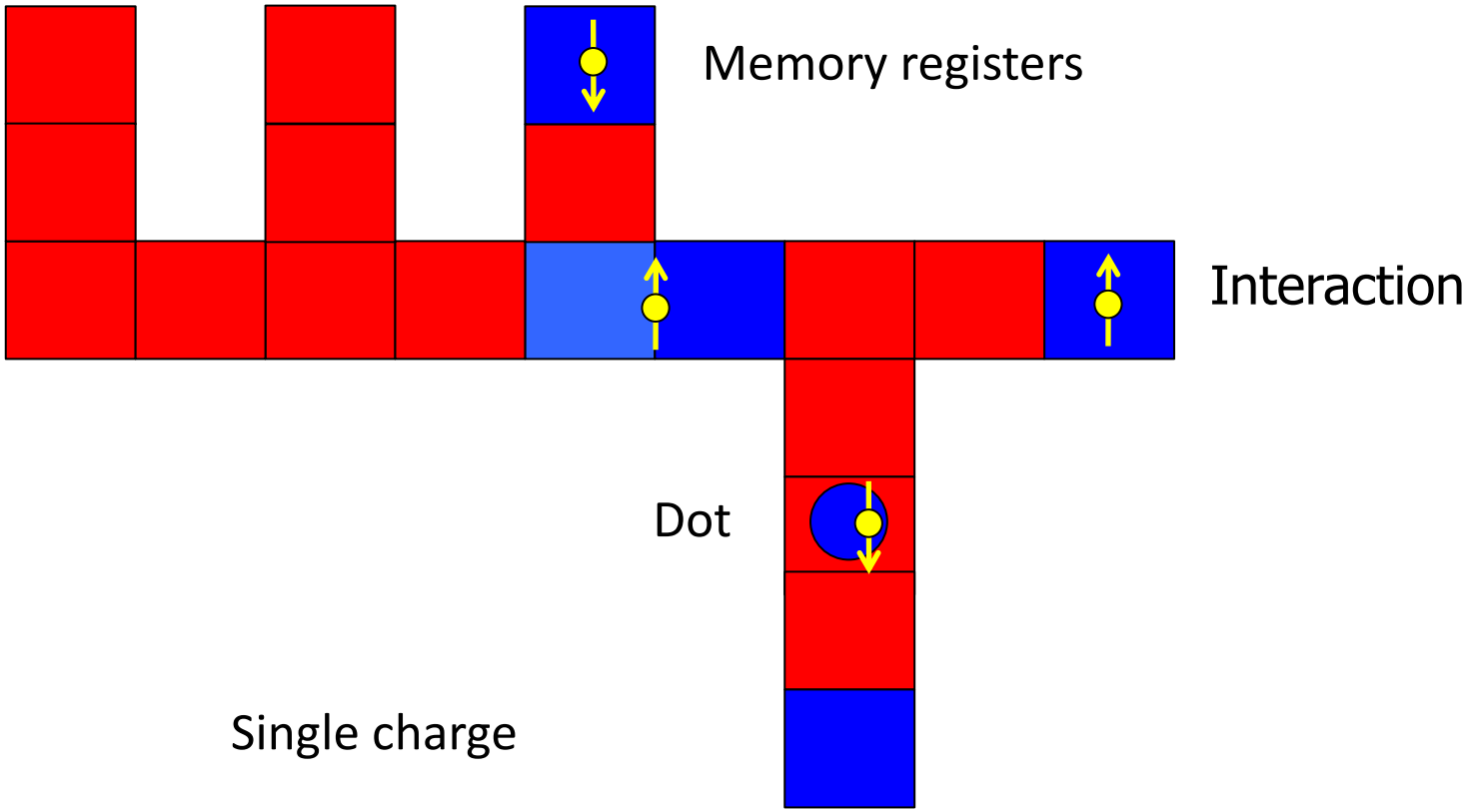

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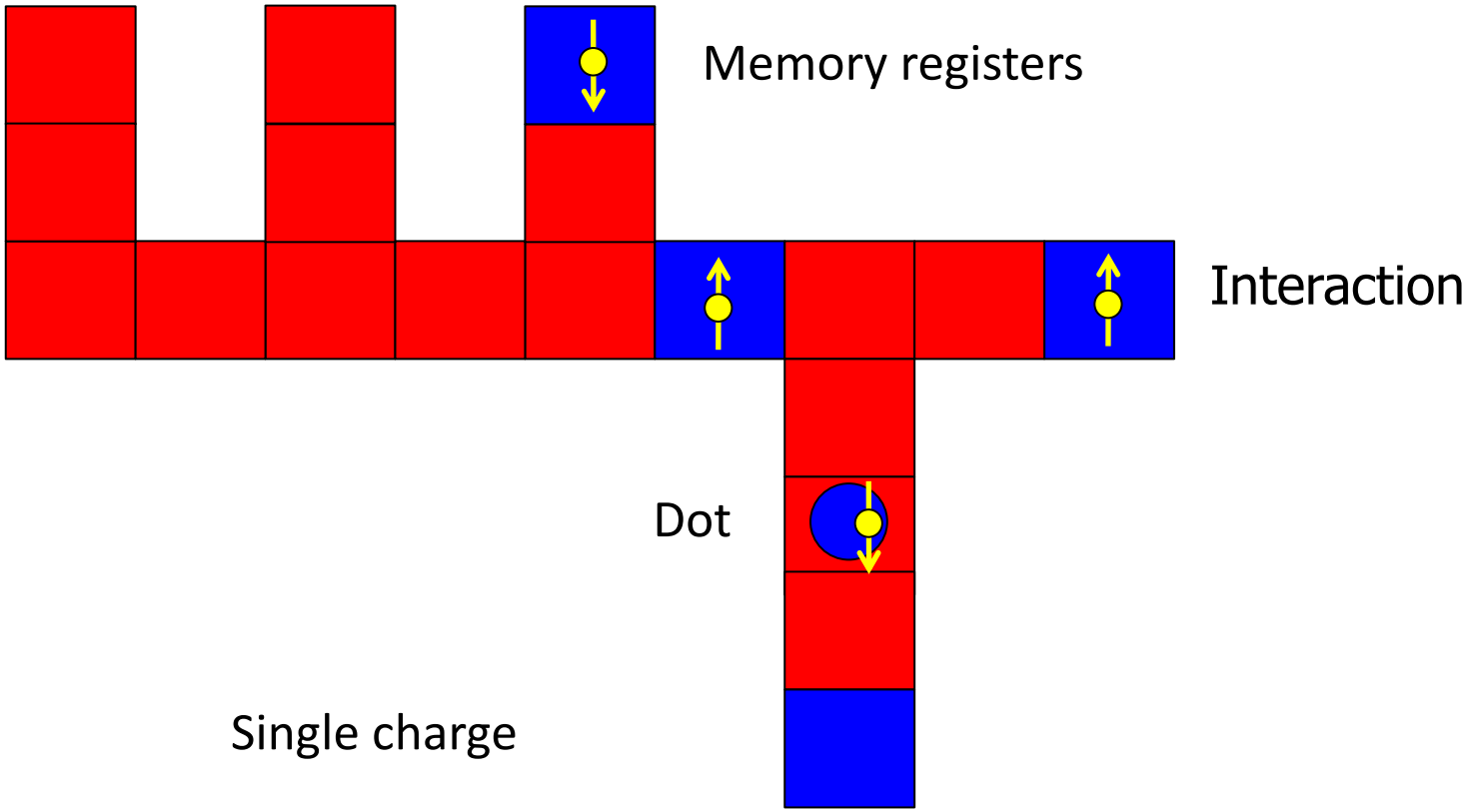

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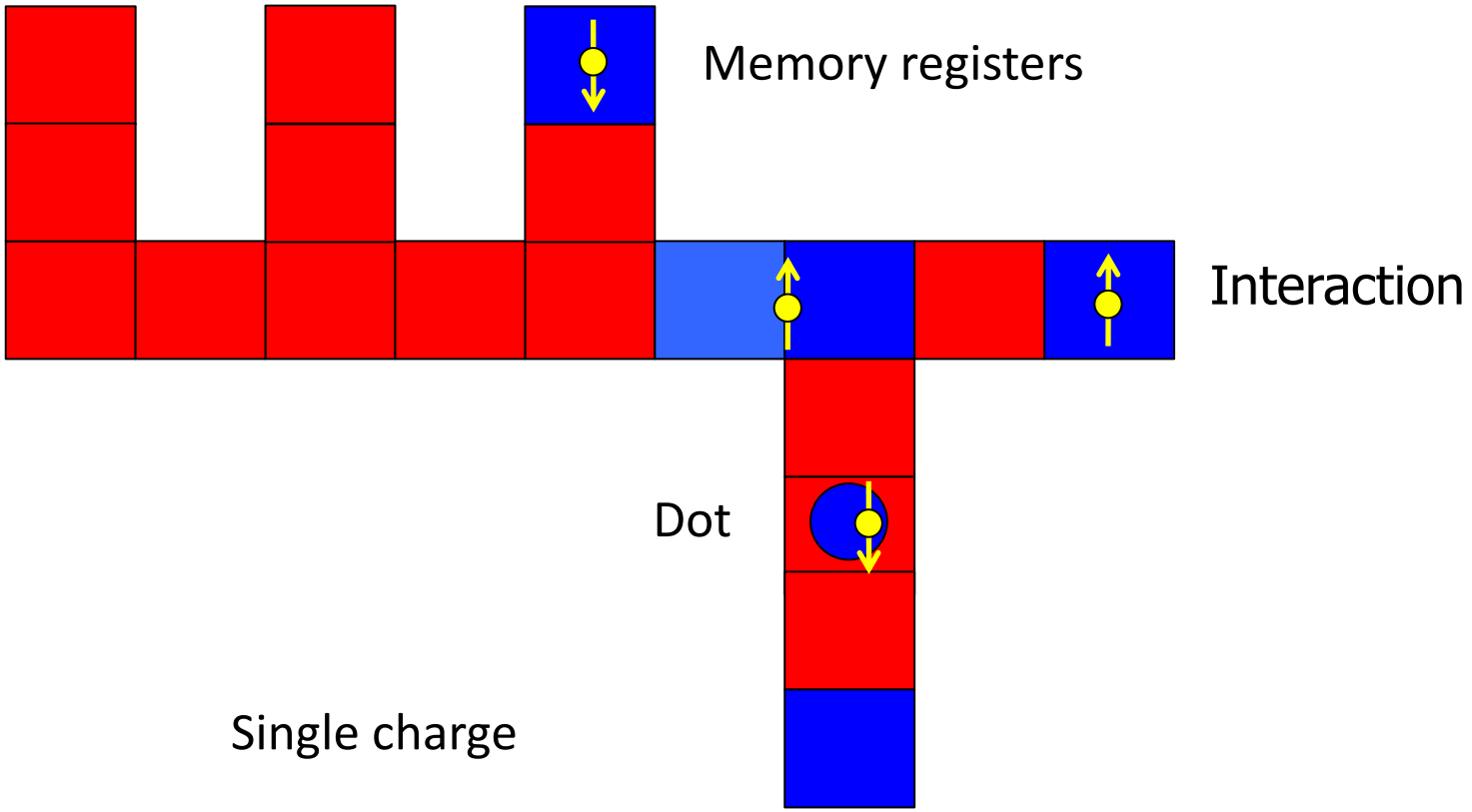

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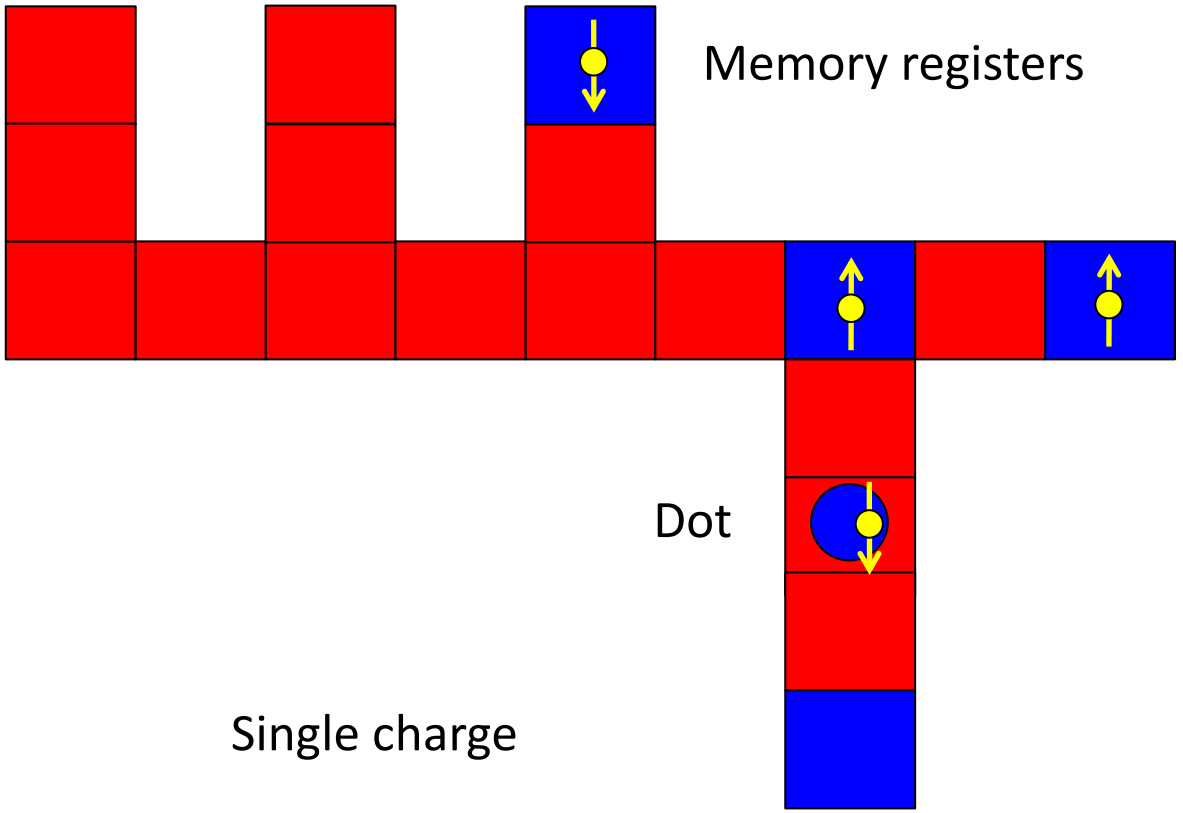

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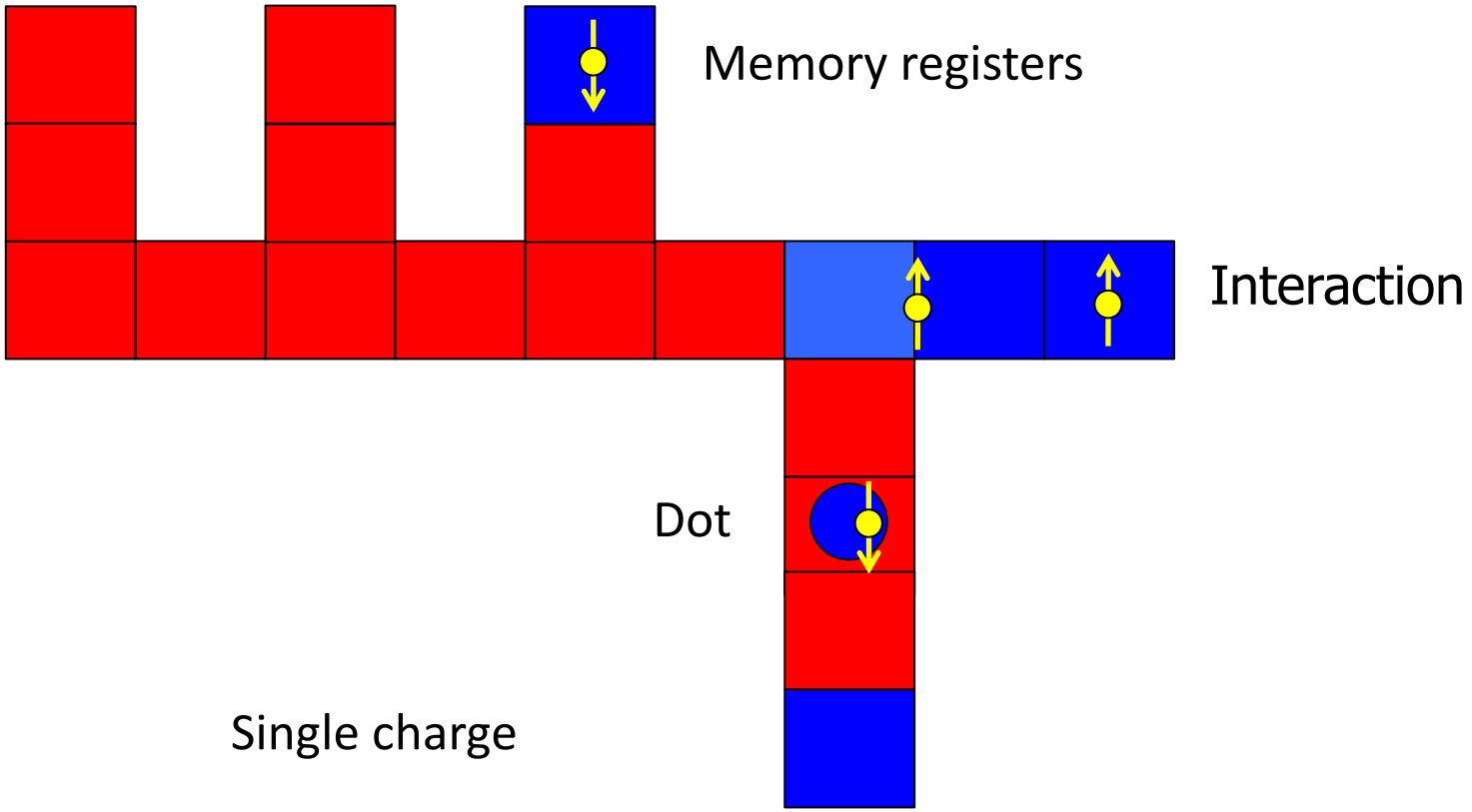

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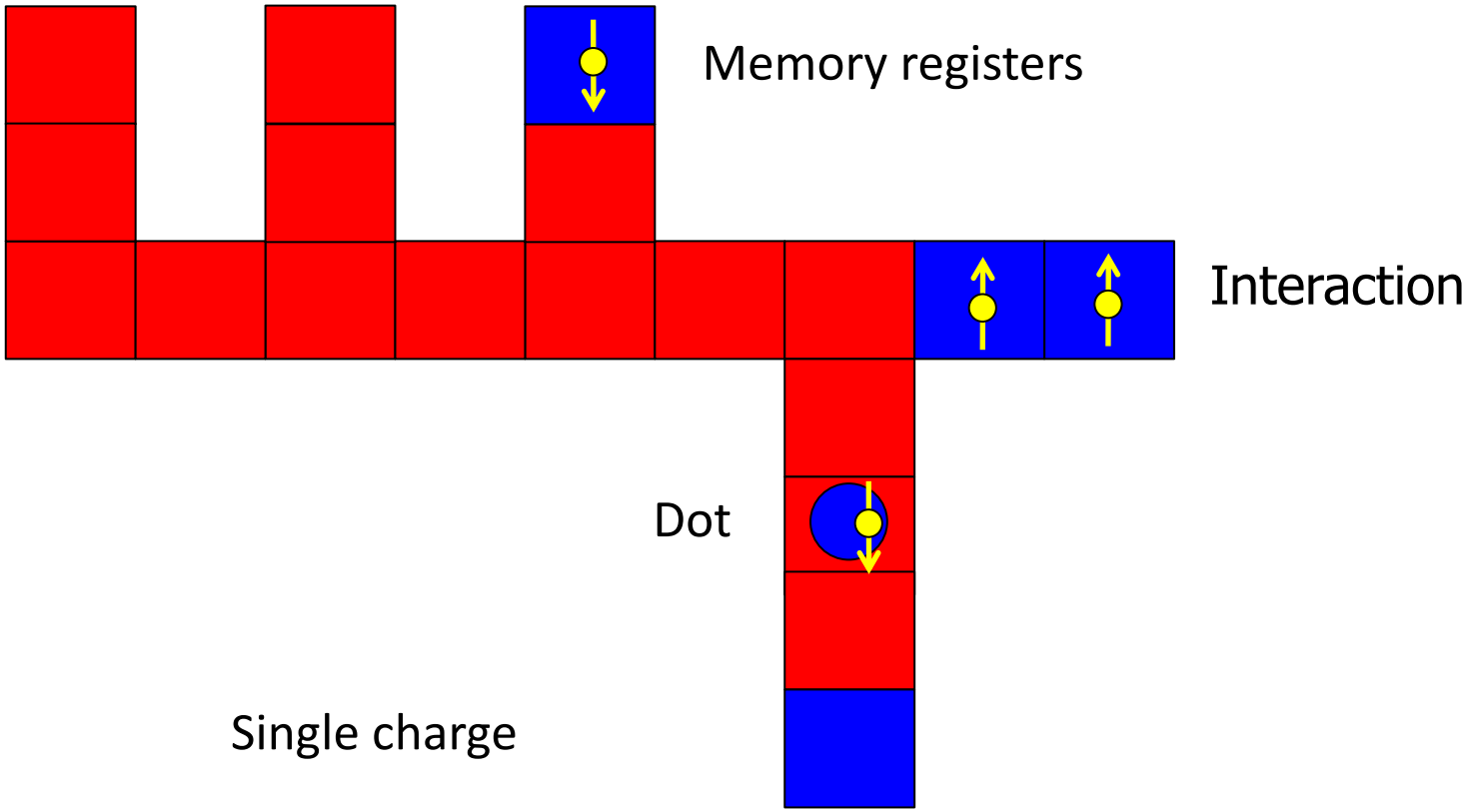

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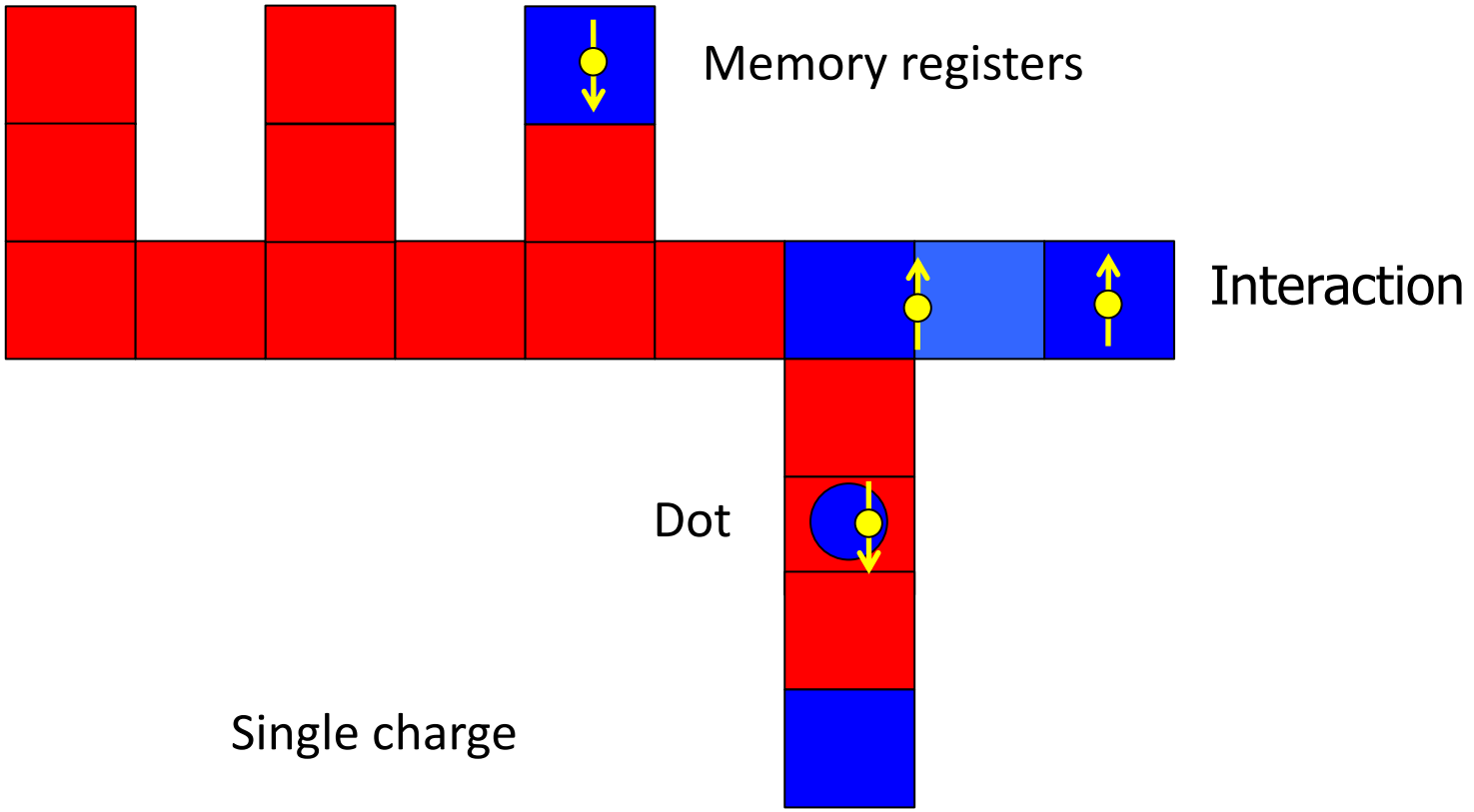

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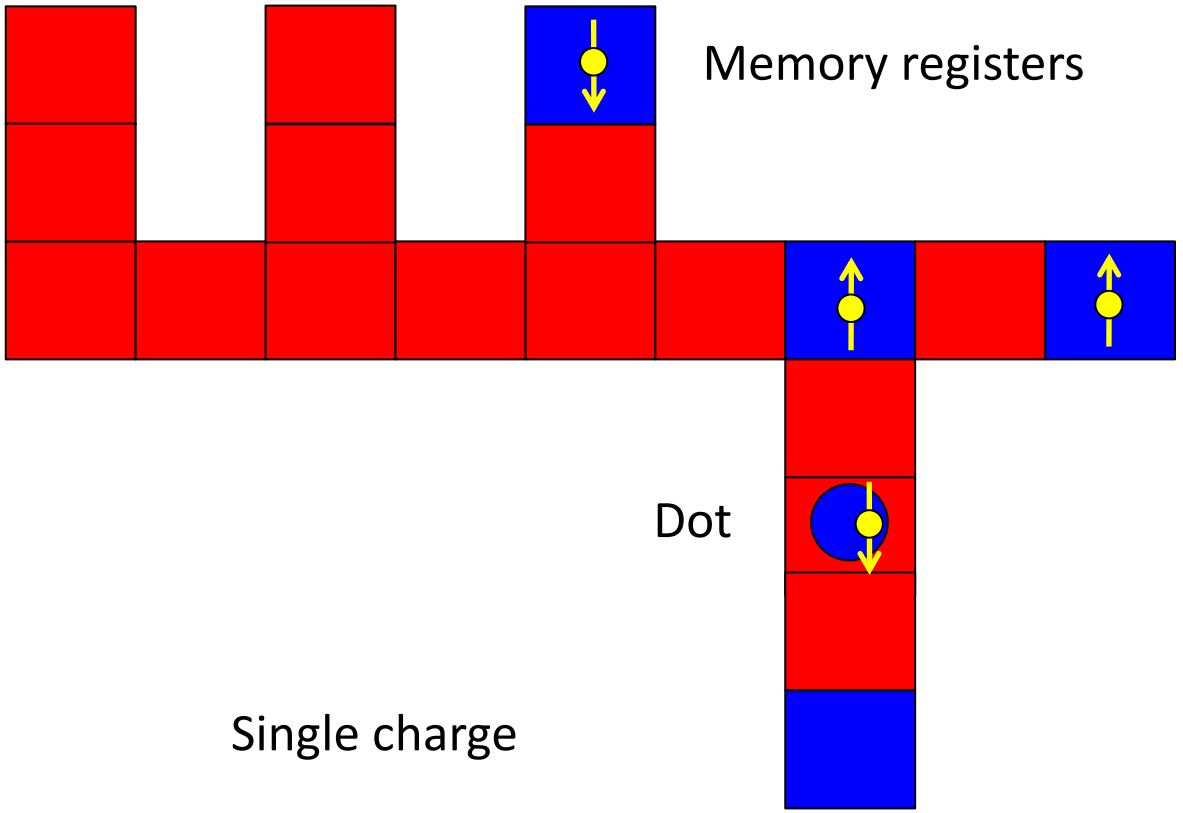

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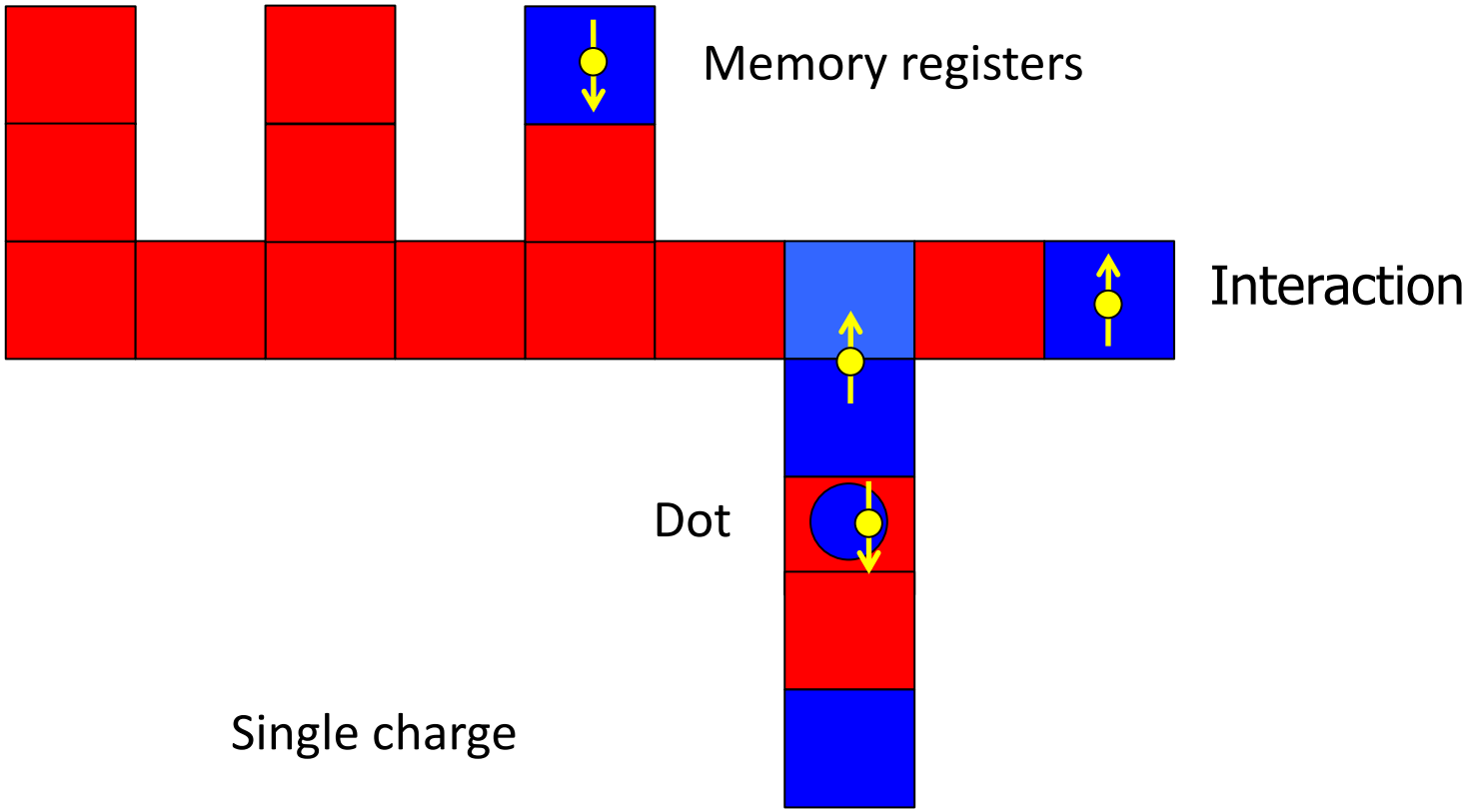

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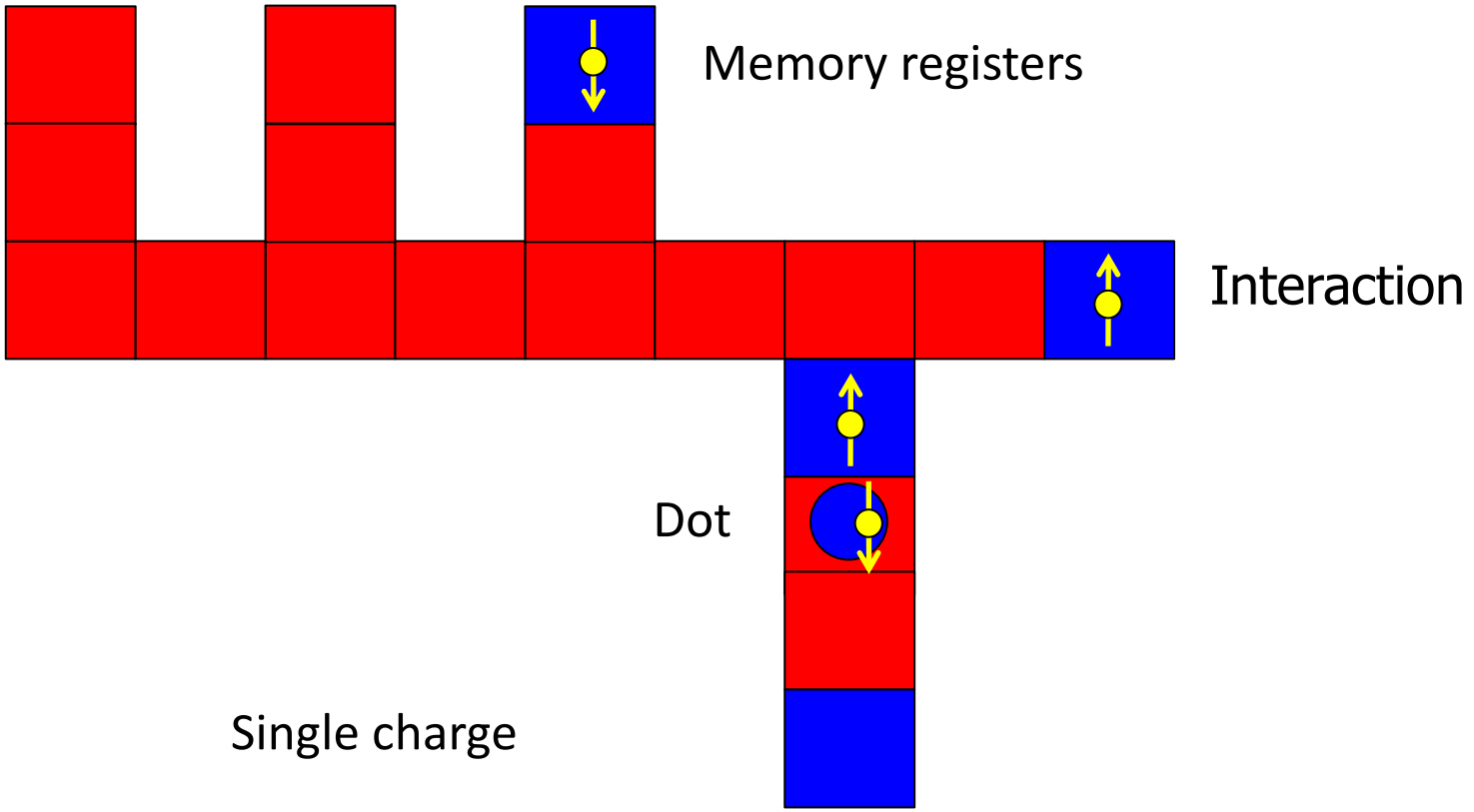

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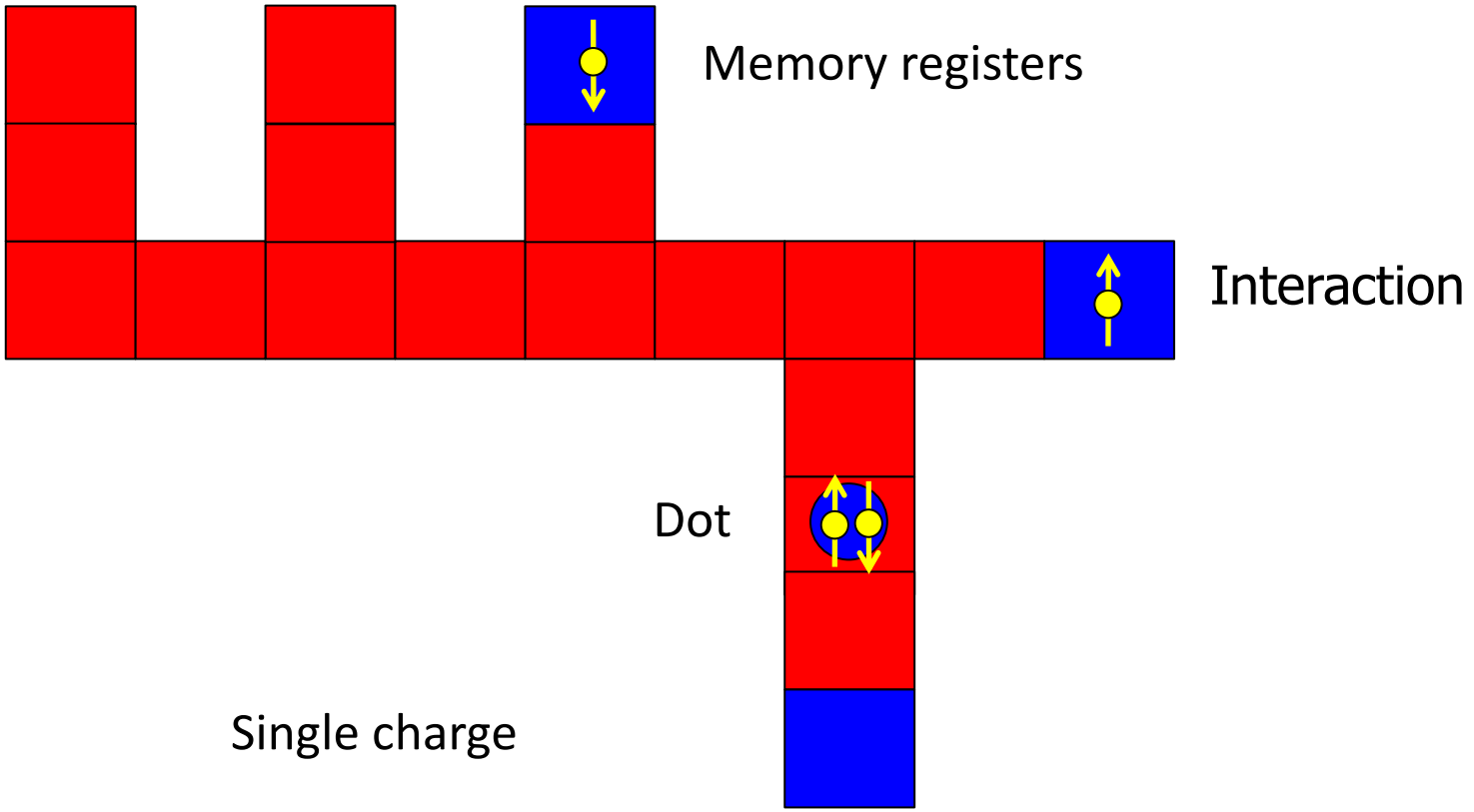

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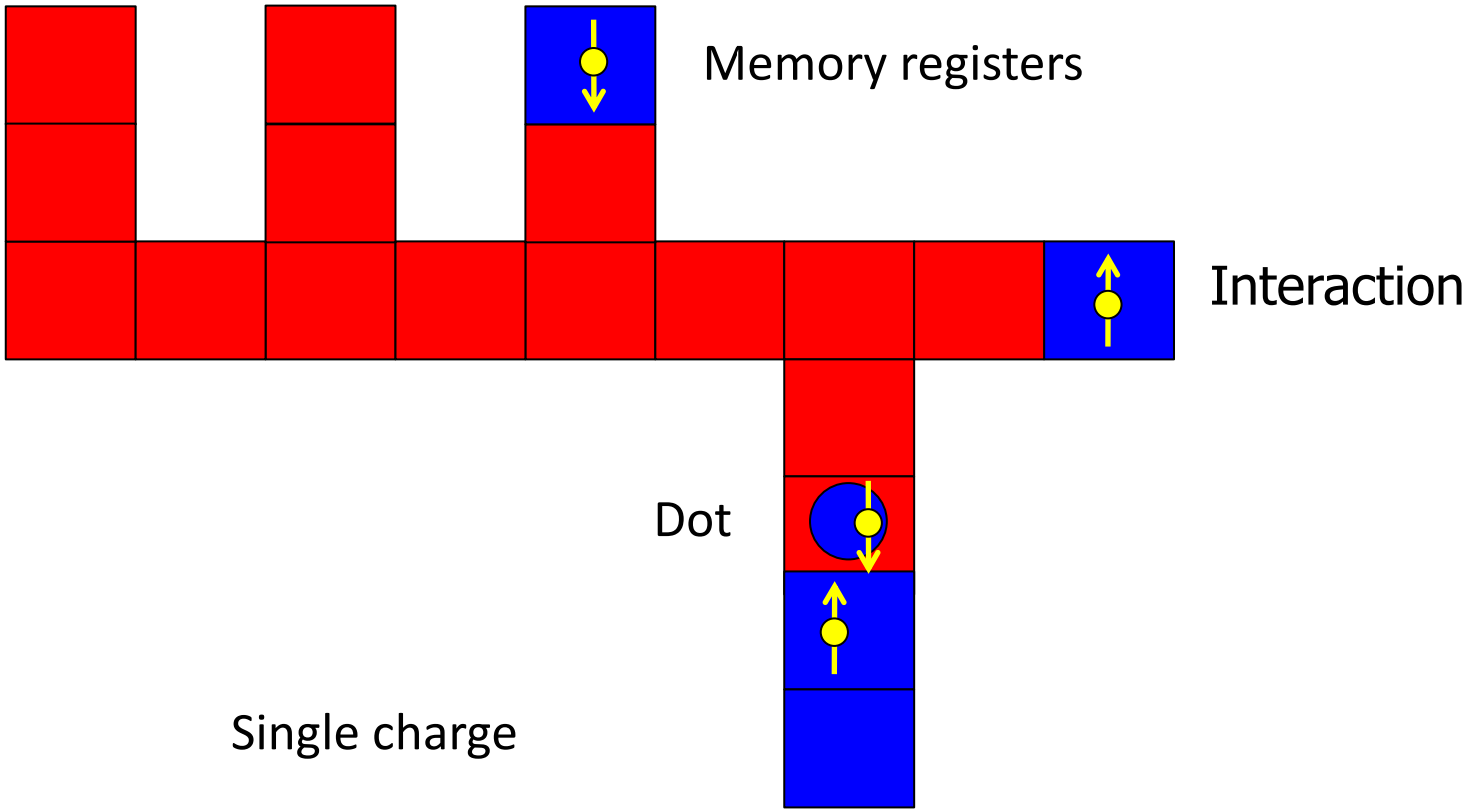

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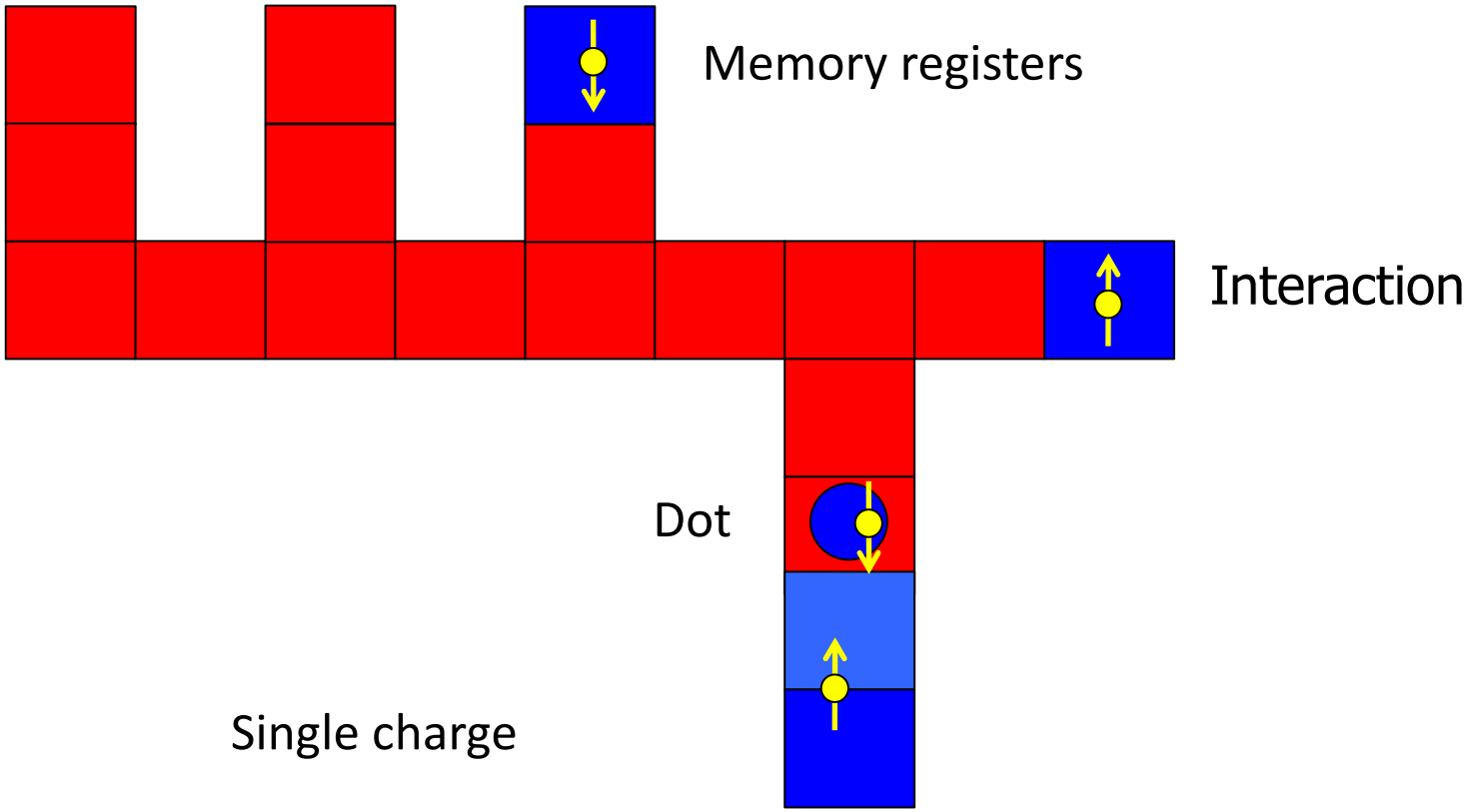

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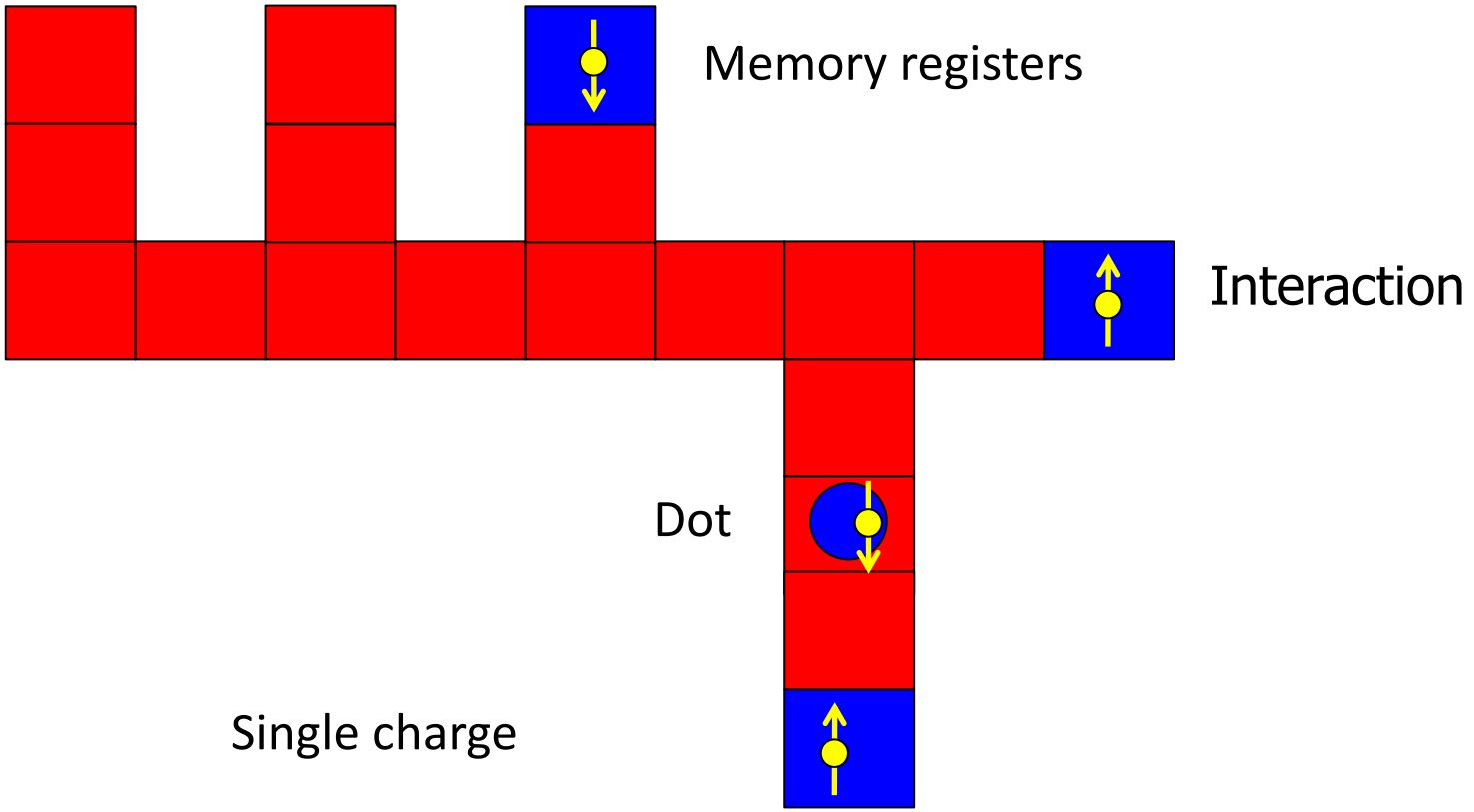
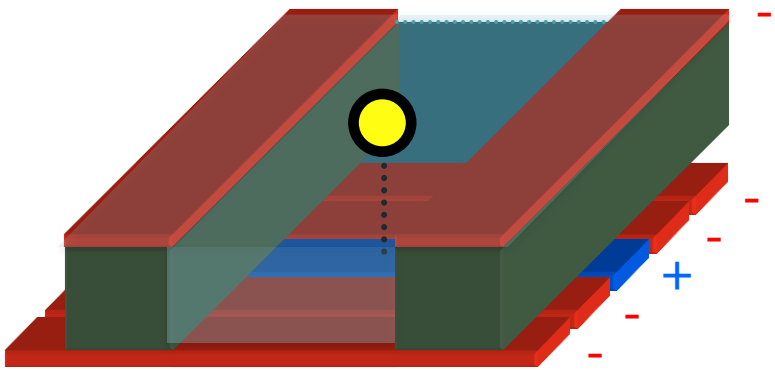
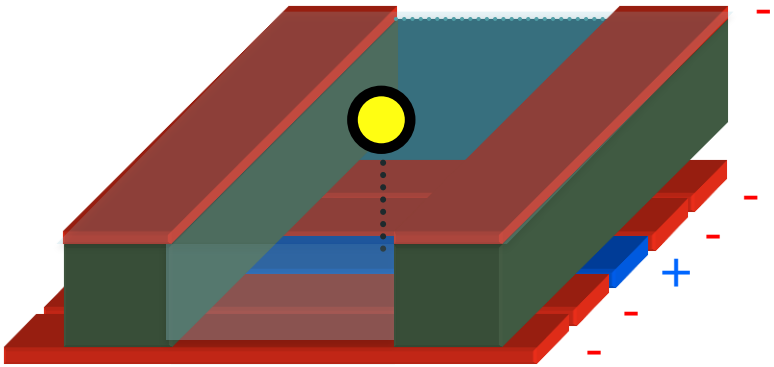
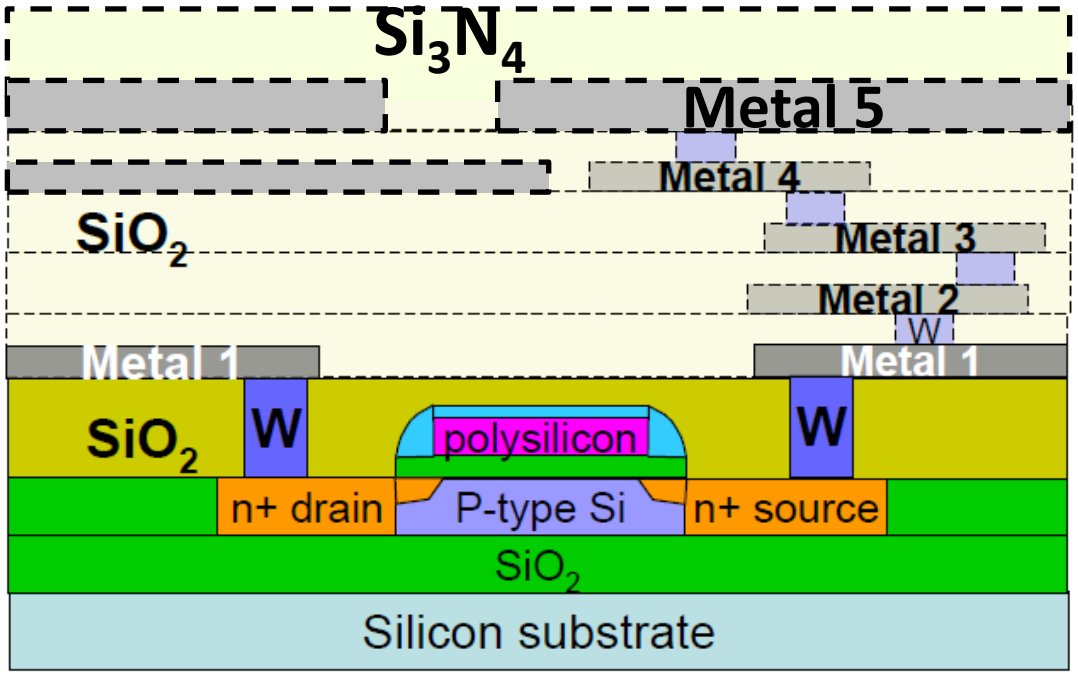


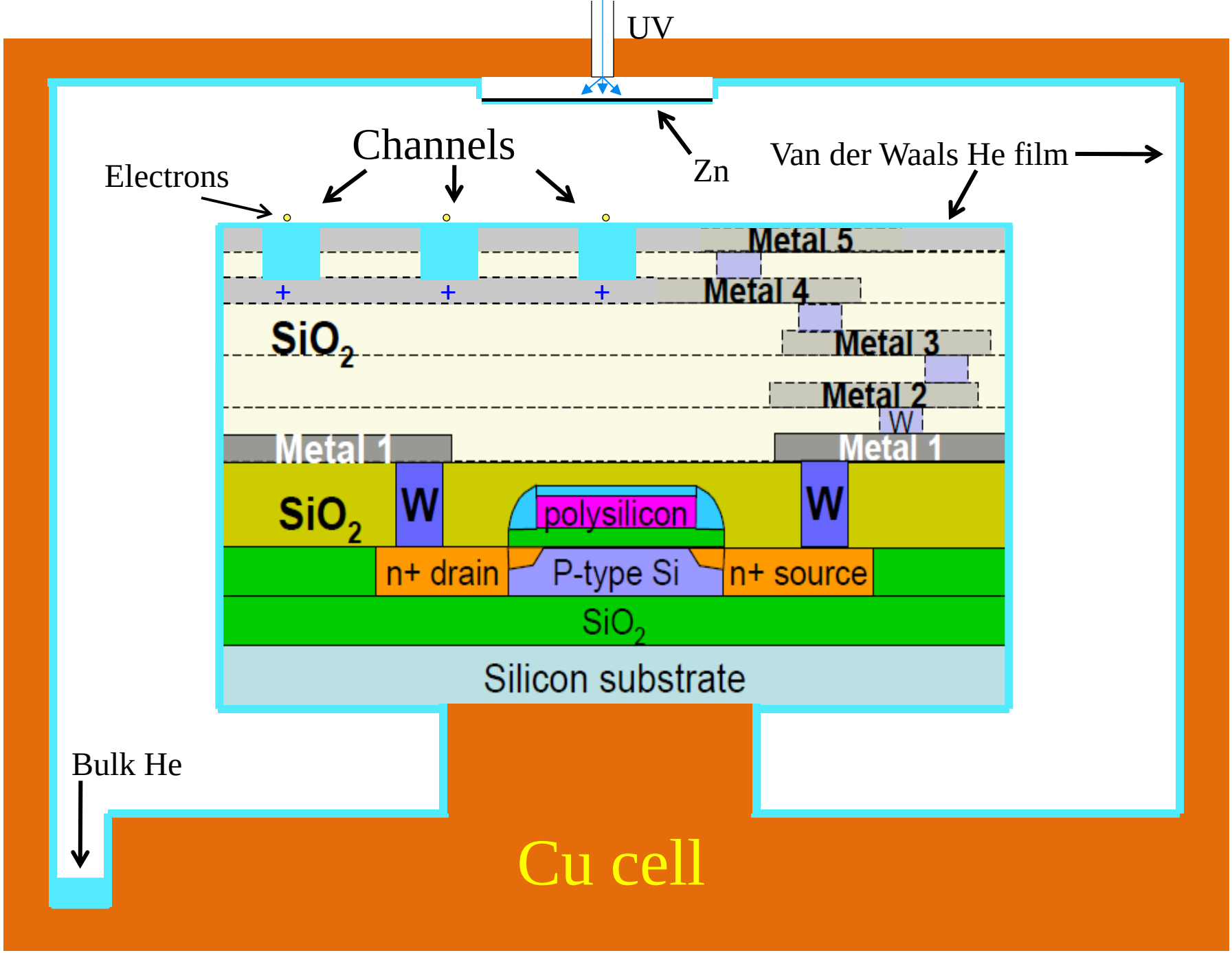
Channel Device with Sandia CMOS7



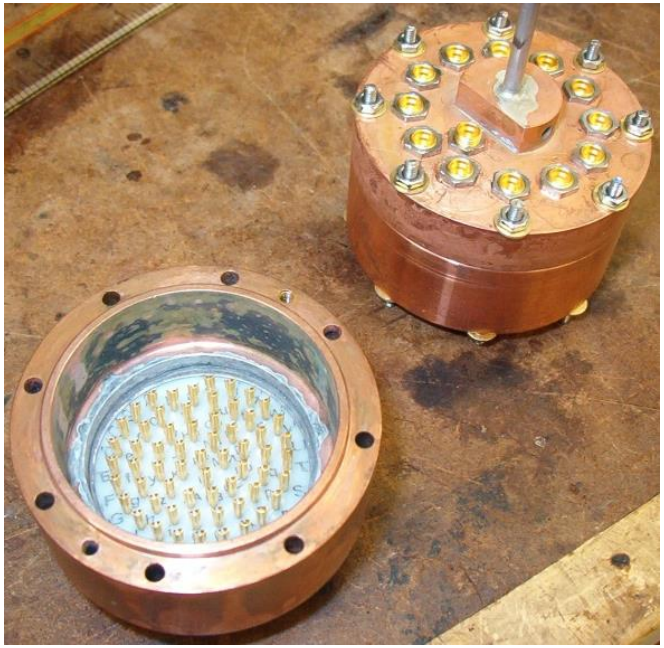
Channel Device with Sandia CMOS7

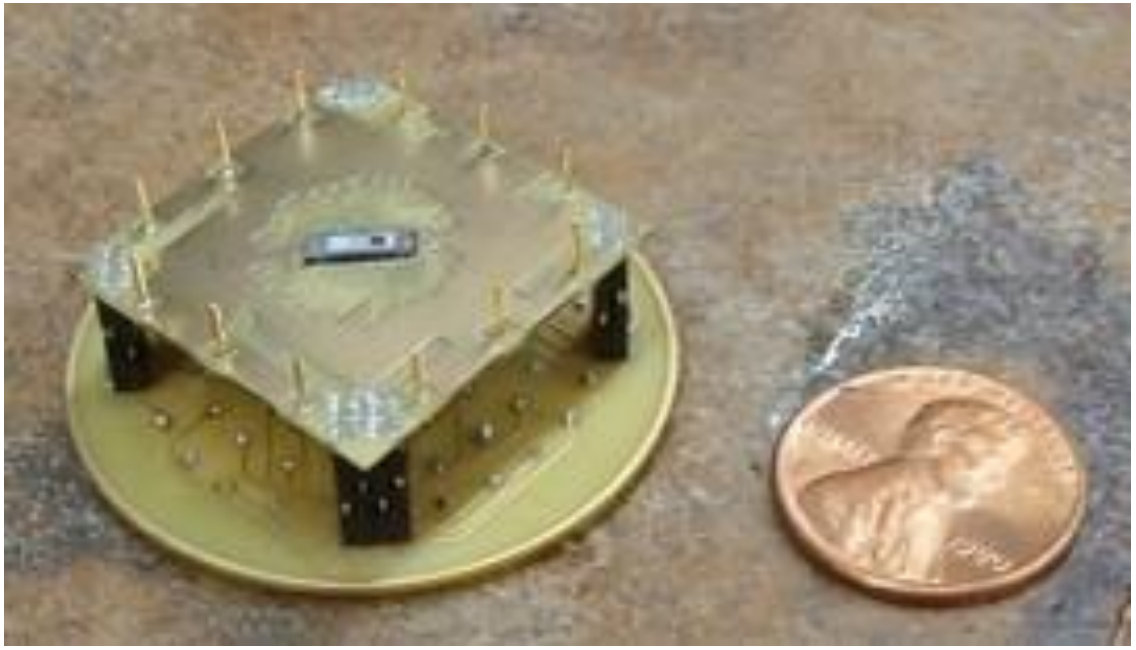




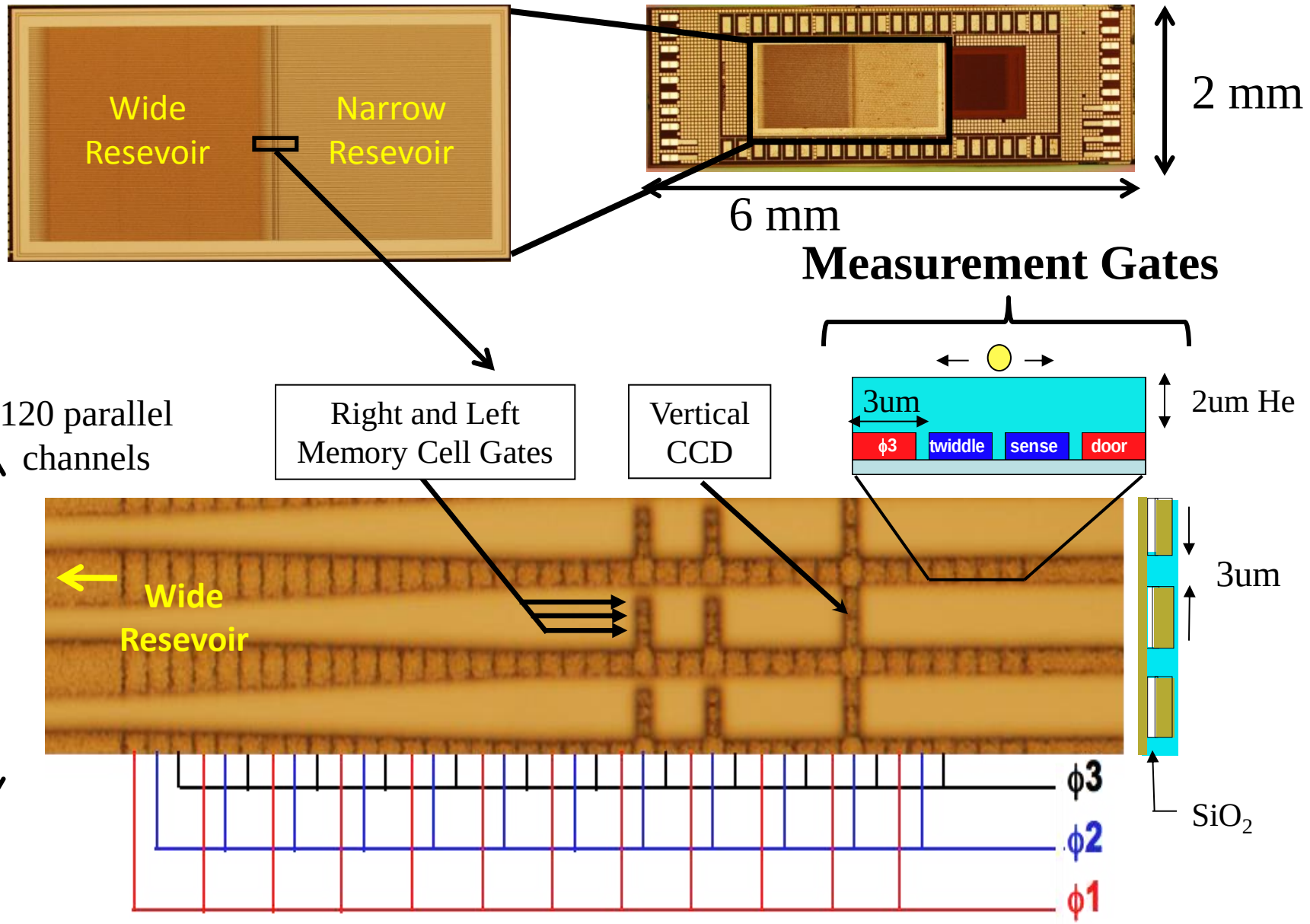

UV
Channels
Electrons
Zn
Van der Waals He film
Metal 5
Metal 4
SiO2
Metal 3
Metal 2
W
Metal 1
Metal 1
SiO2
W
polysilicon
W
n+ drain
P-type Si
n+ source
SiO2
Silicon substrate
Bulk He
Cu cell

Experiment



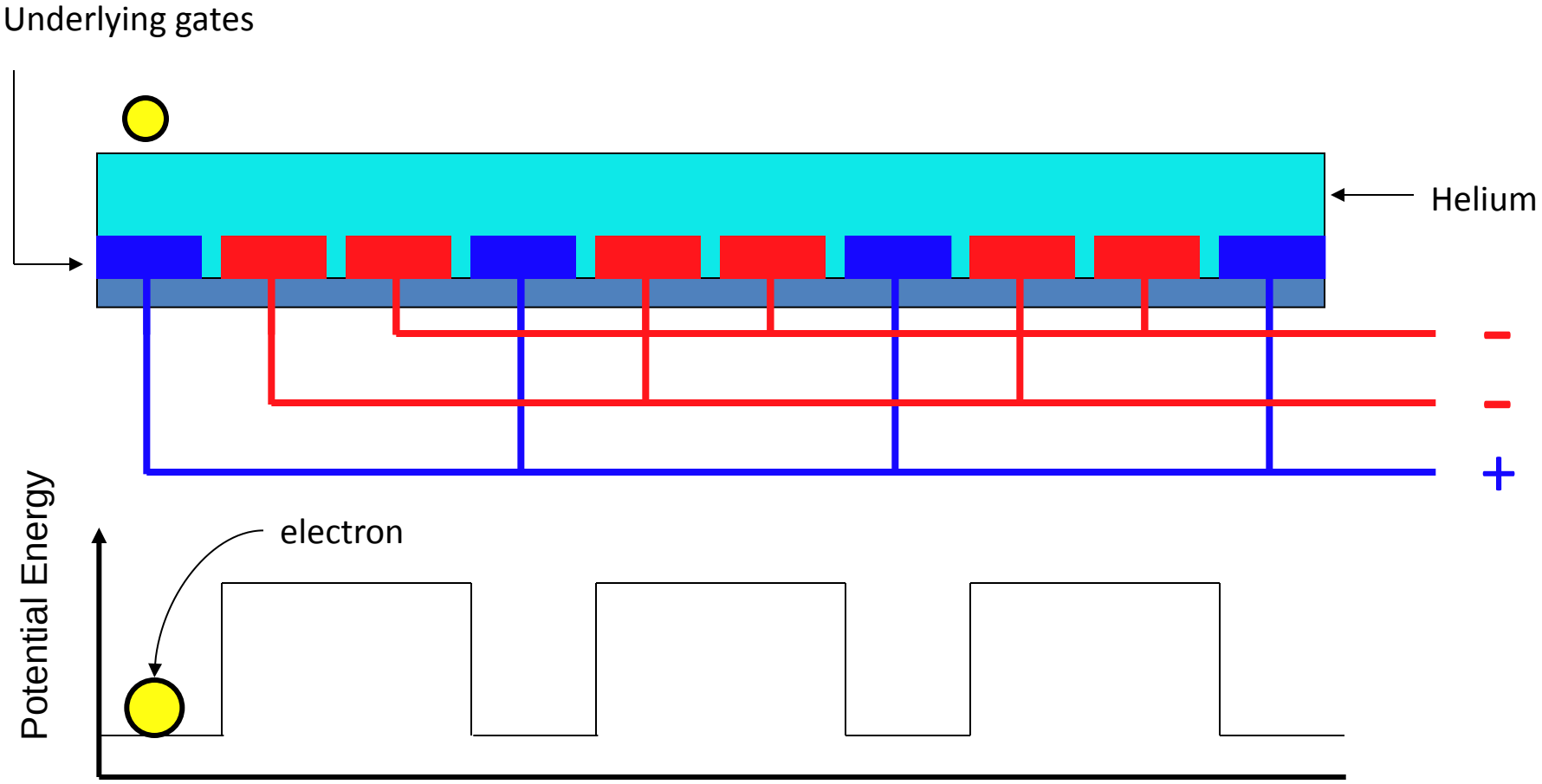


Sandia Device



3-phase CCD

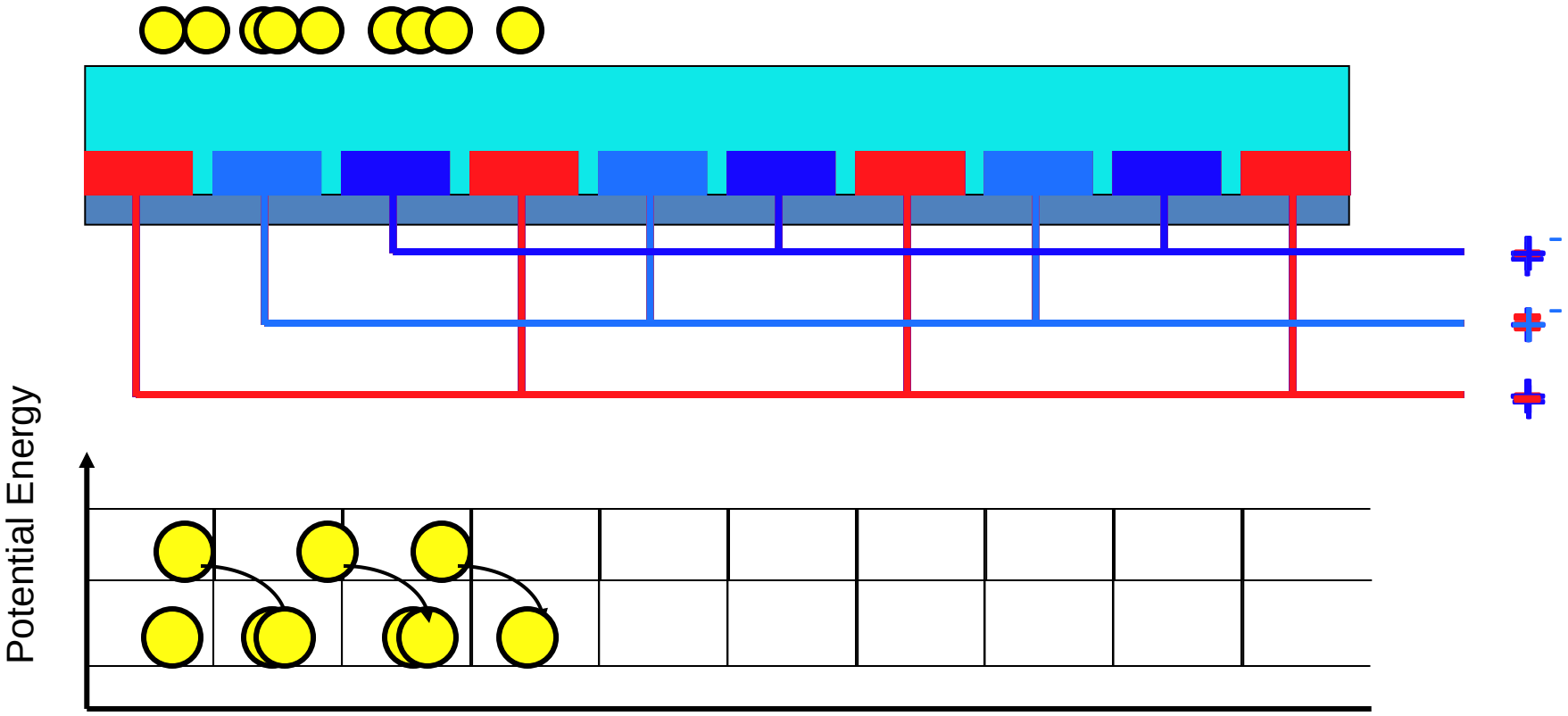
Potential

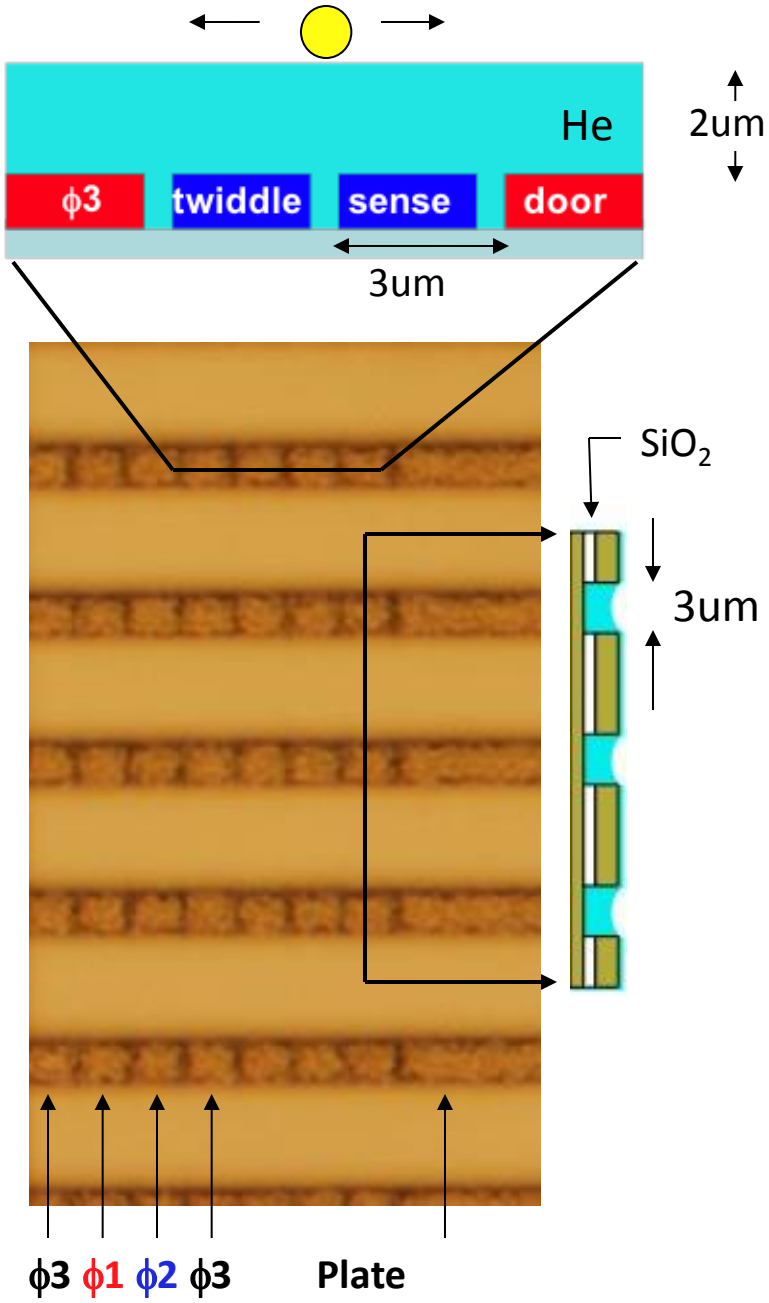


3-phase CCD

Clocking #3

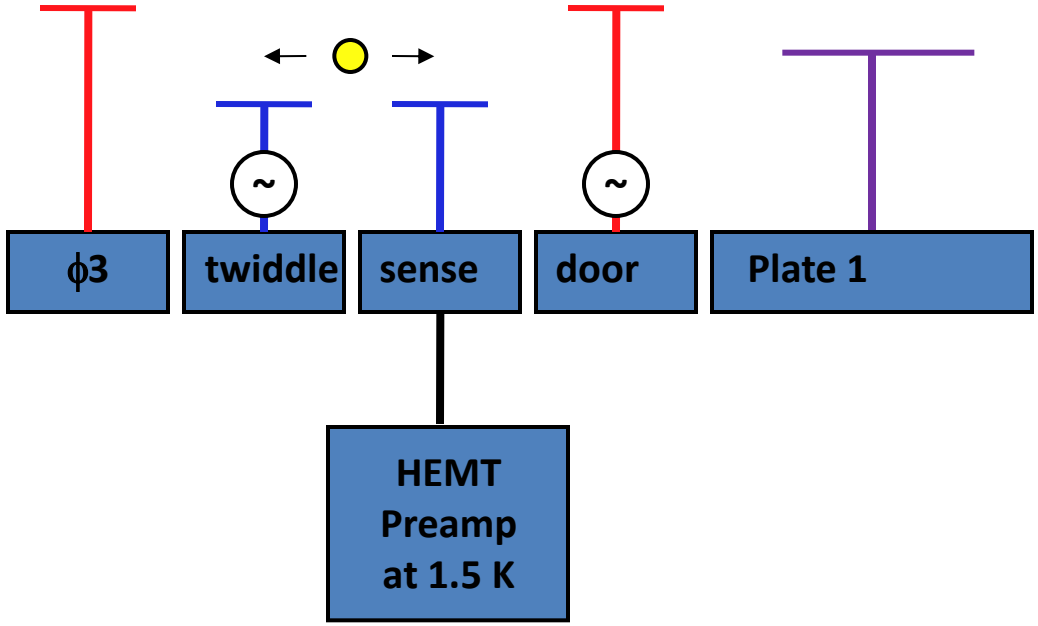
Electron has moved one pixel (3 gates) to the right





Measurement

Modulate twiddle to push electron on and off the sense gate



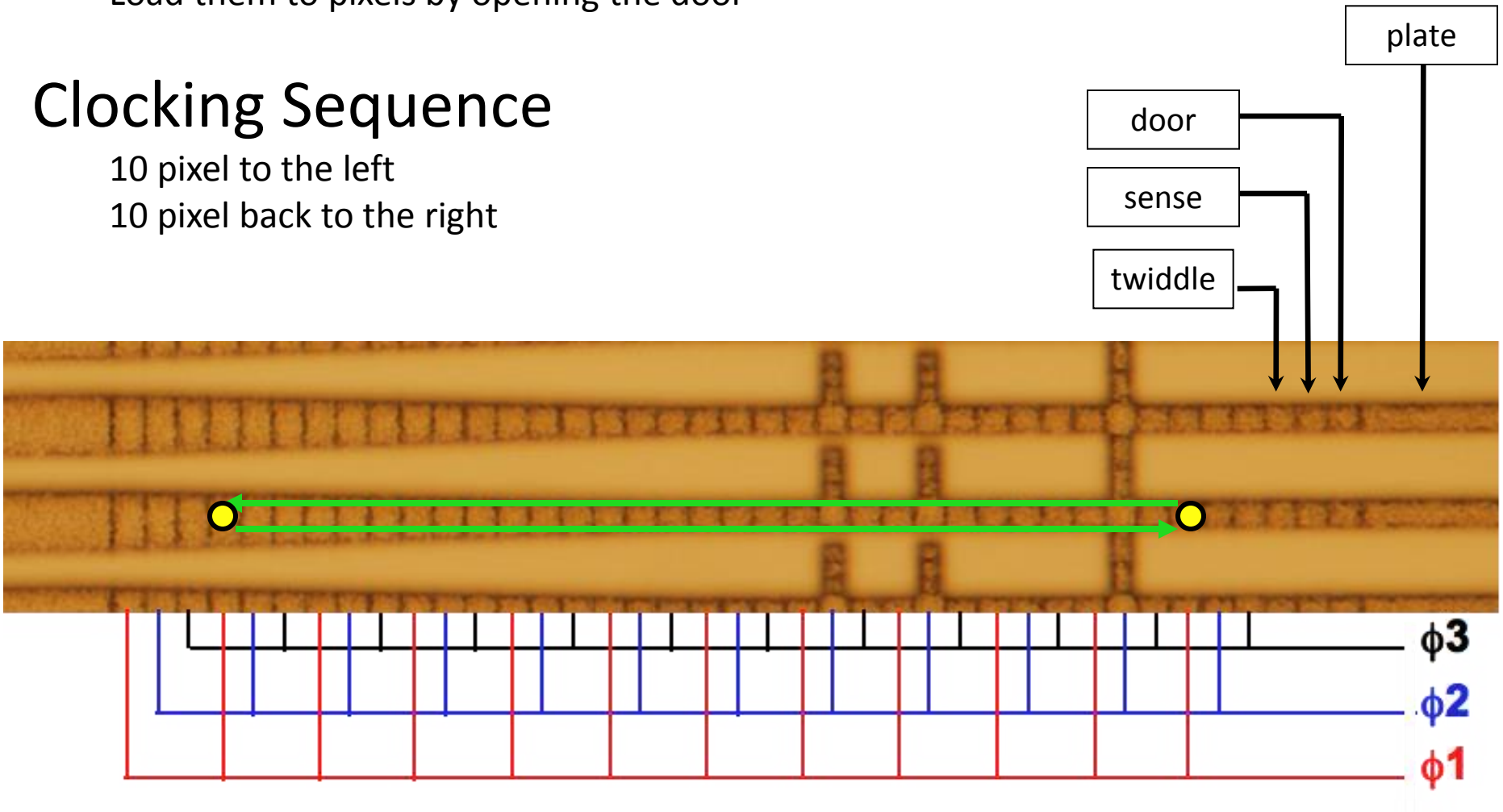
Horizontal CCD

Loading:

Photoemit electrons on plates
Load them to pixels by opening the door

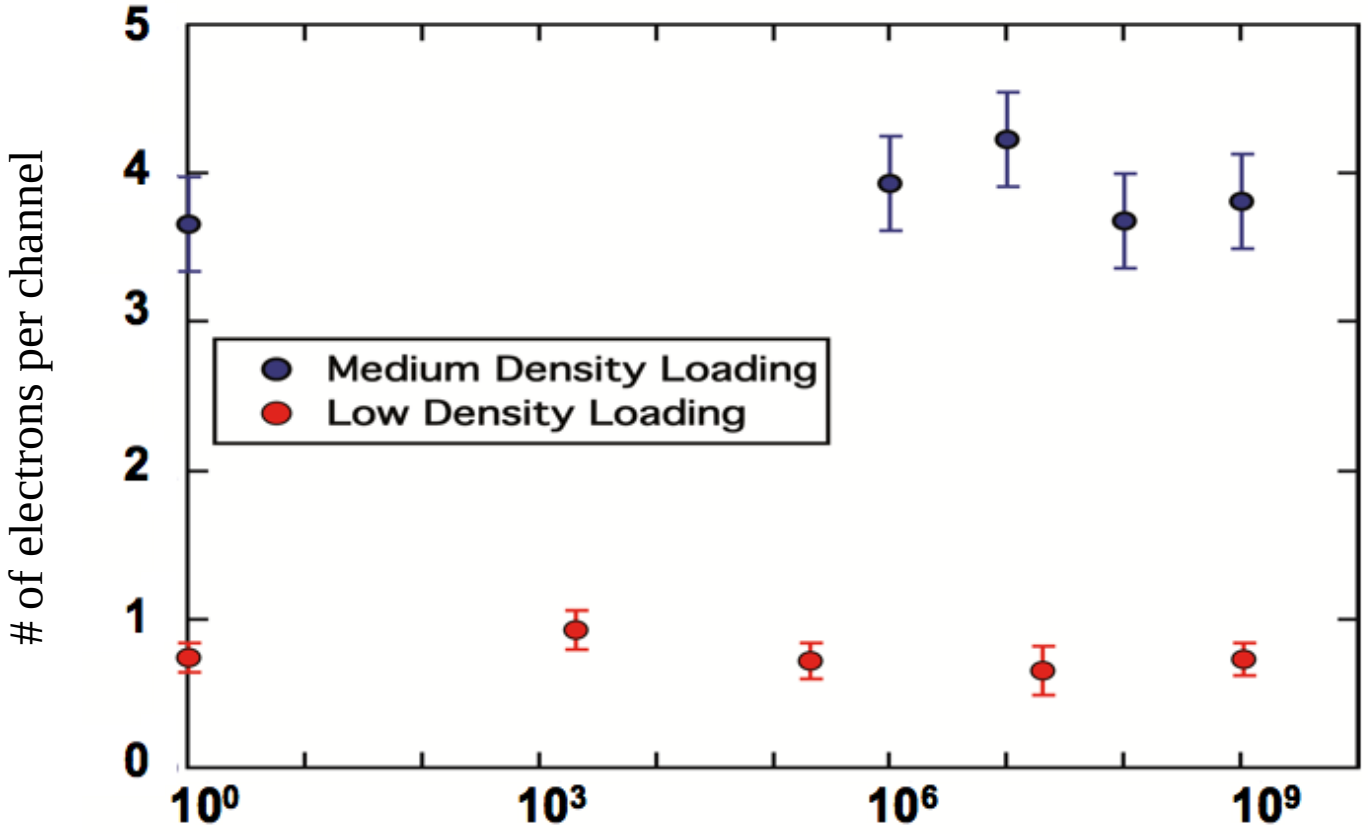
Clocking Sequence

10 pixel to the left
10 pixel back to the right



Horizontal Clocking Efficiency

Clock (pixel) rate = 240kHz

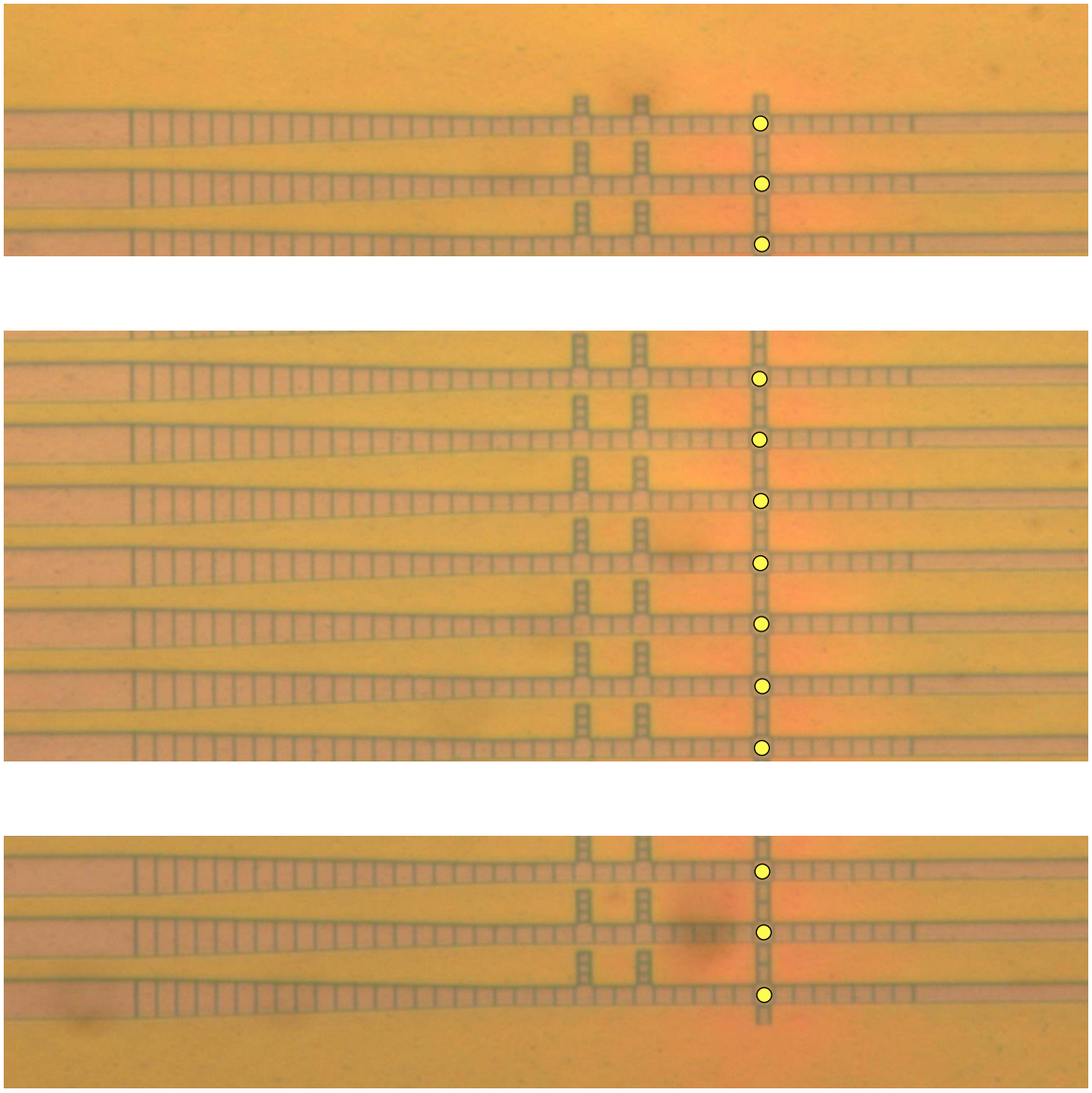


~ 70 min.

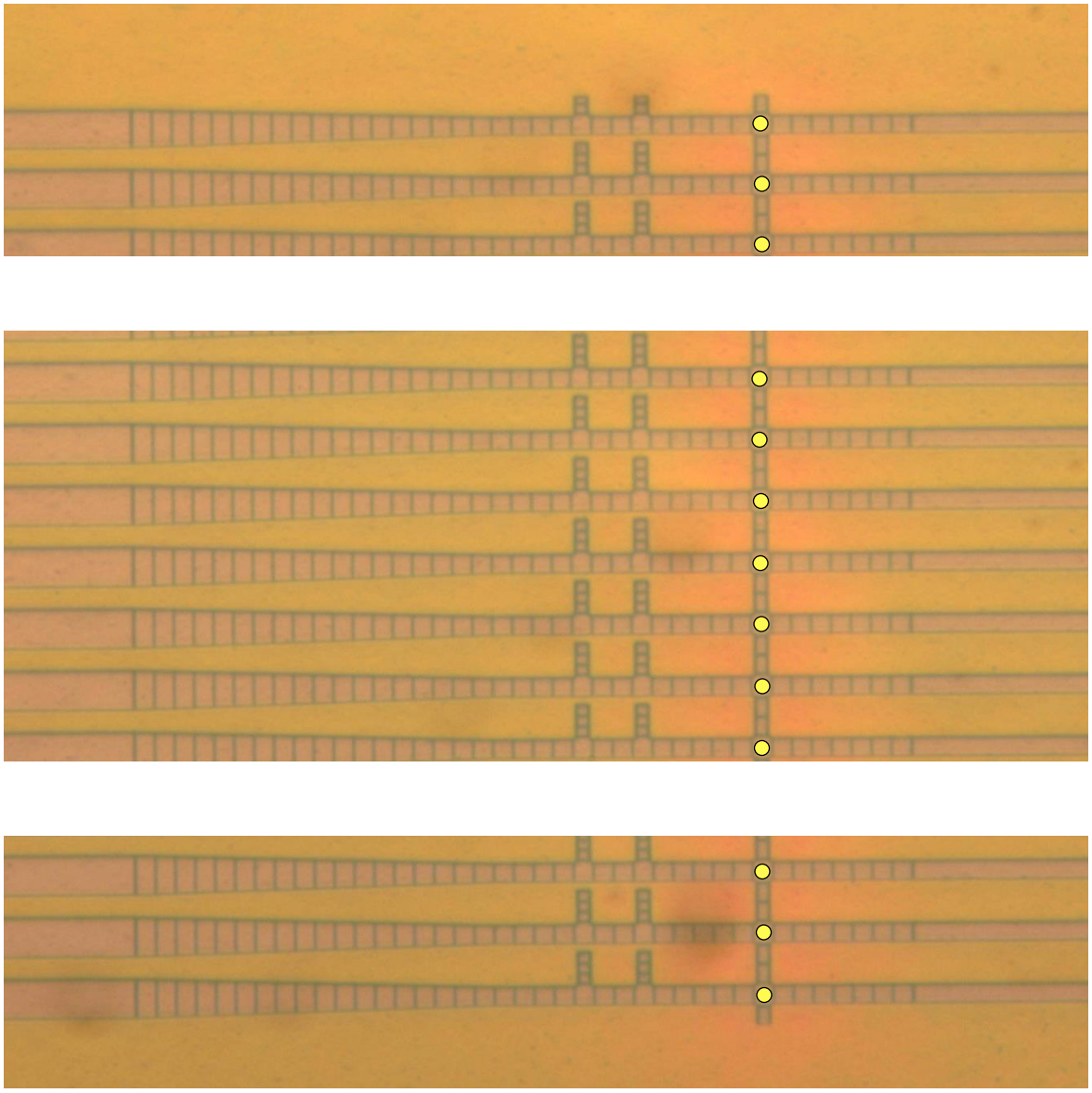
~ 9 km.

No measurable errors

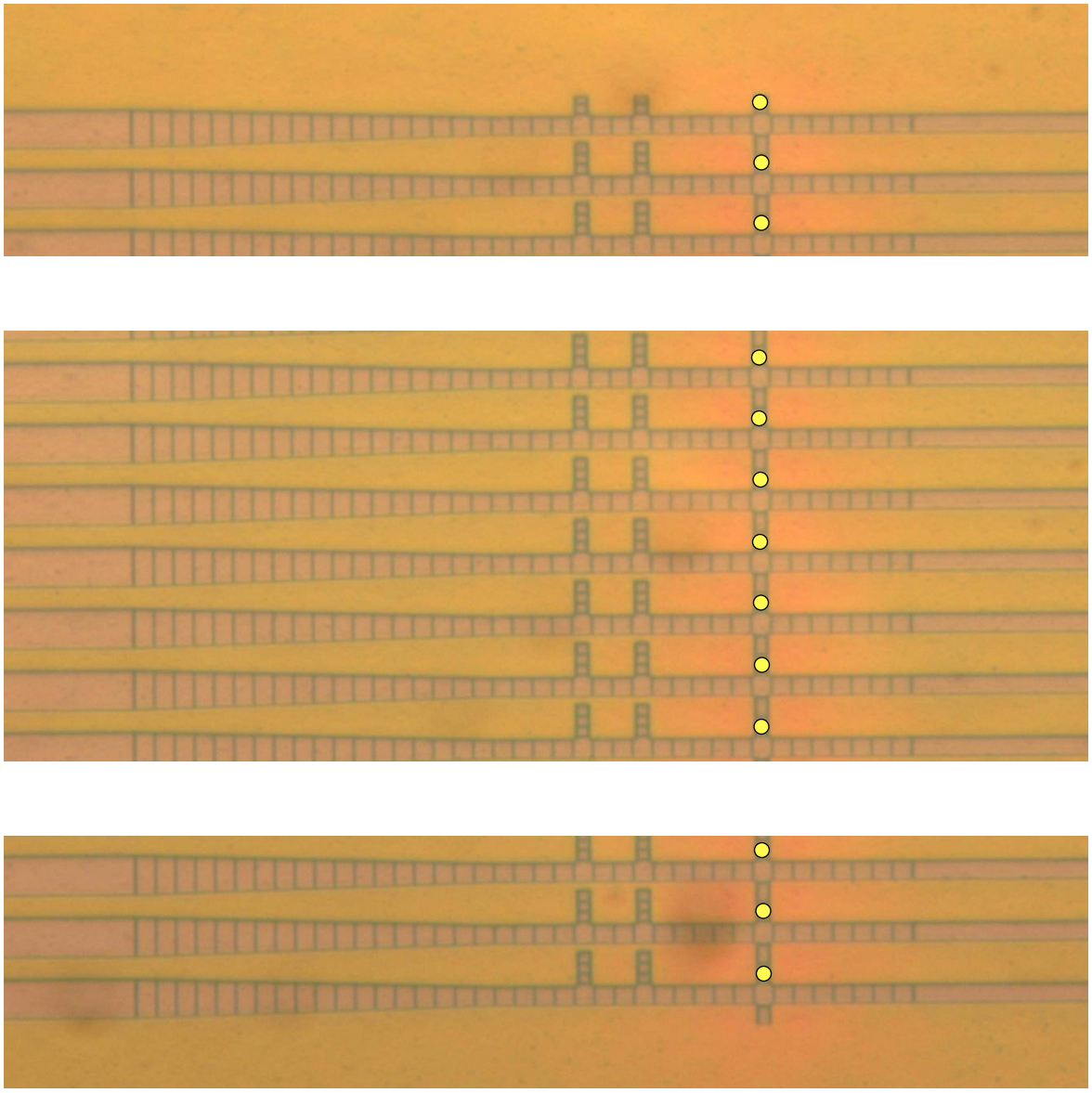
Vertical Clocking



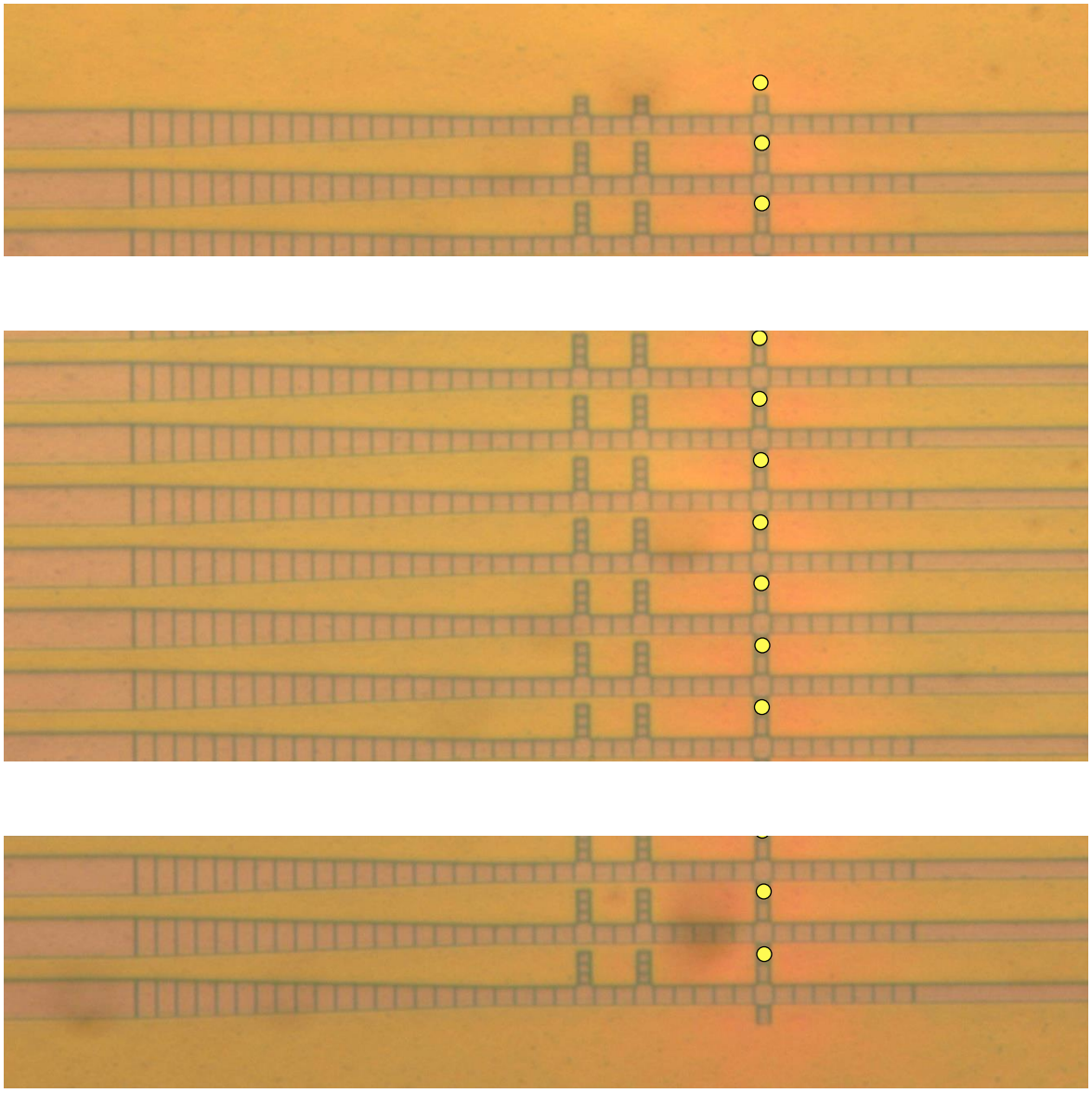
Vertical Clocking



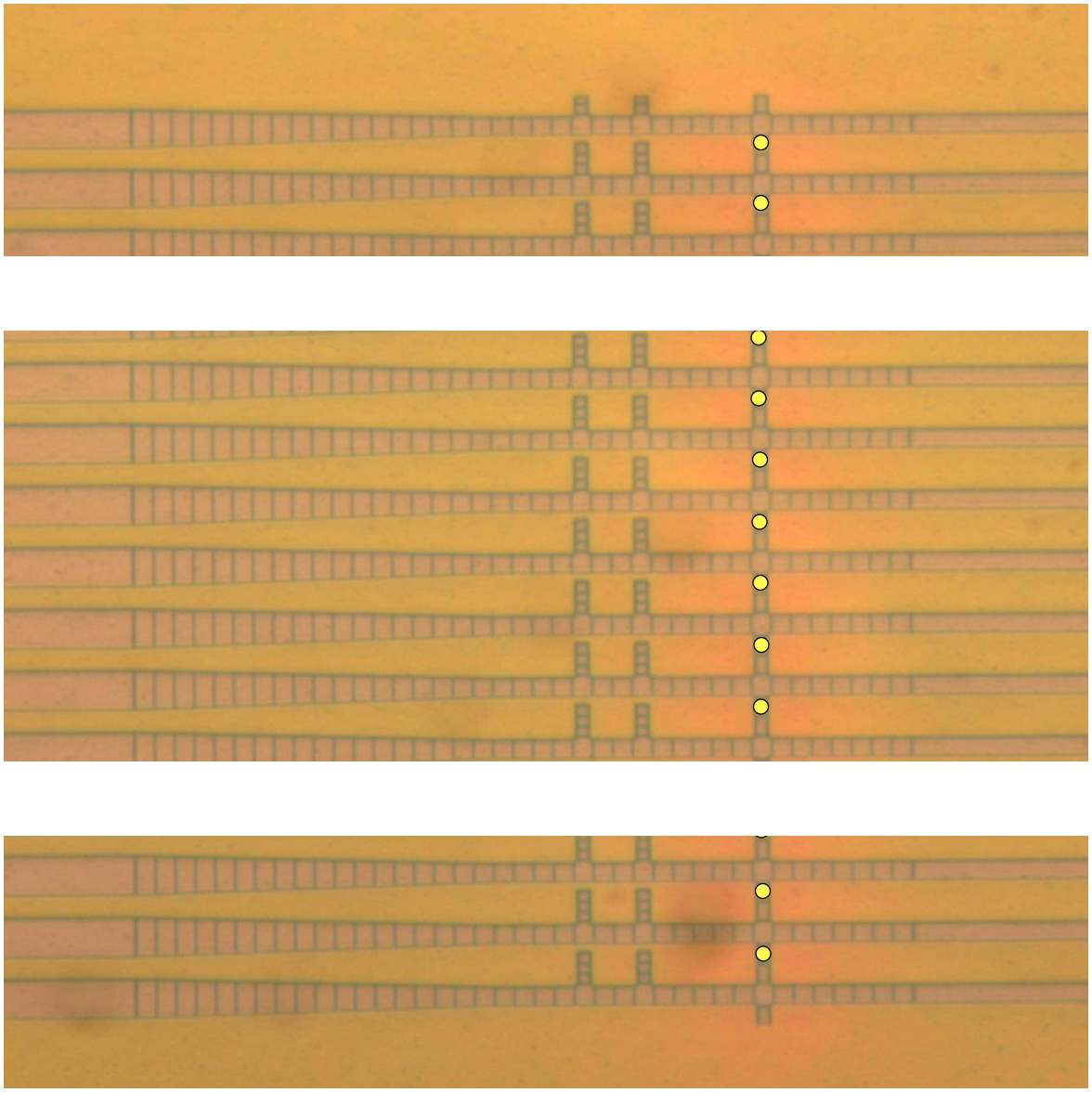
Vertical Clocking



Vertical Clocking



Vertical Clocking



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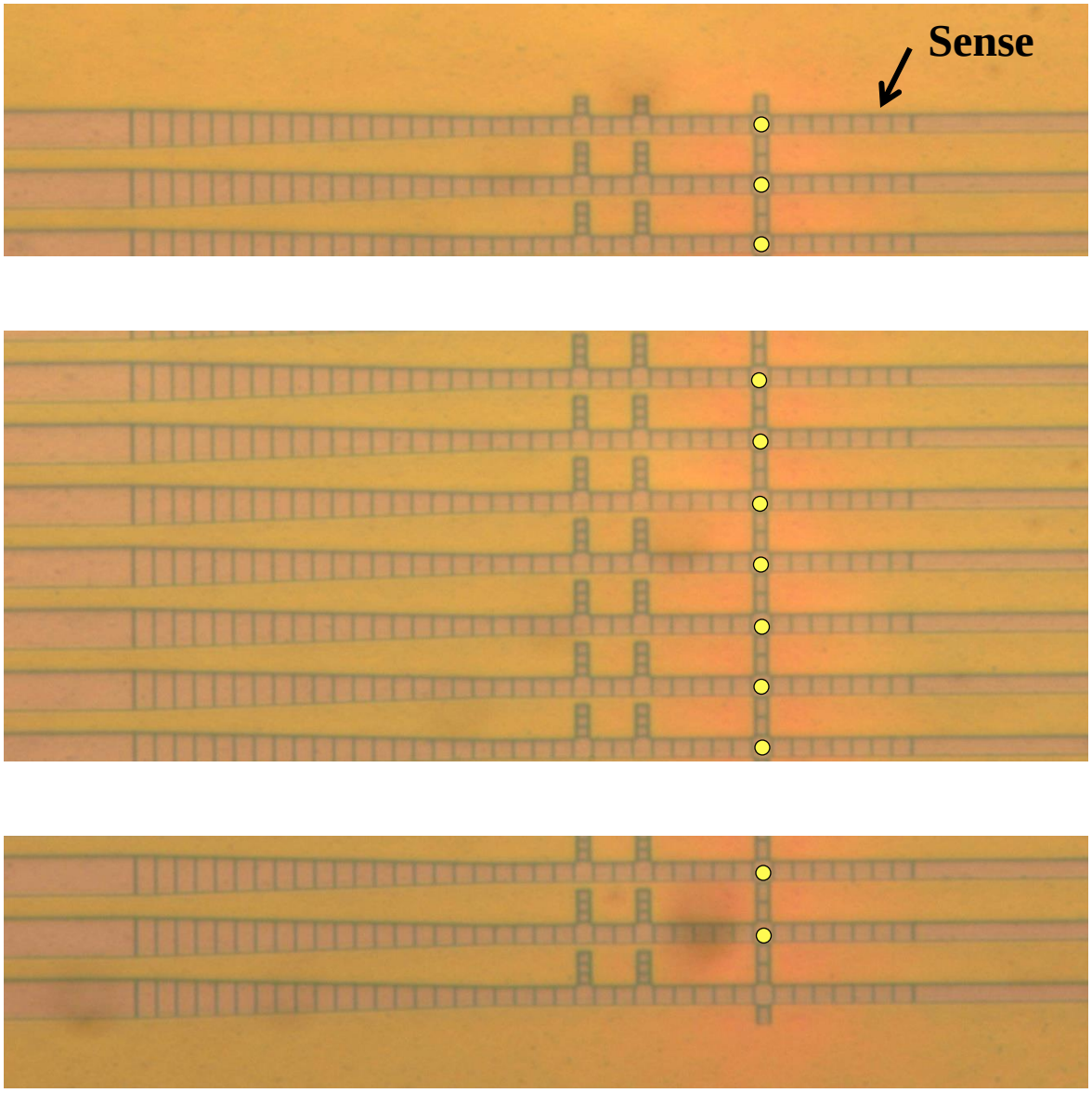
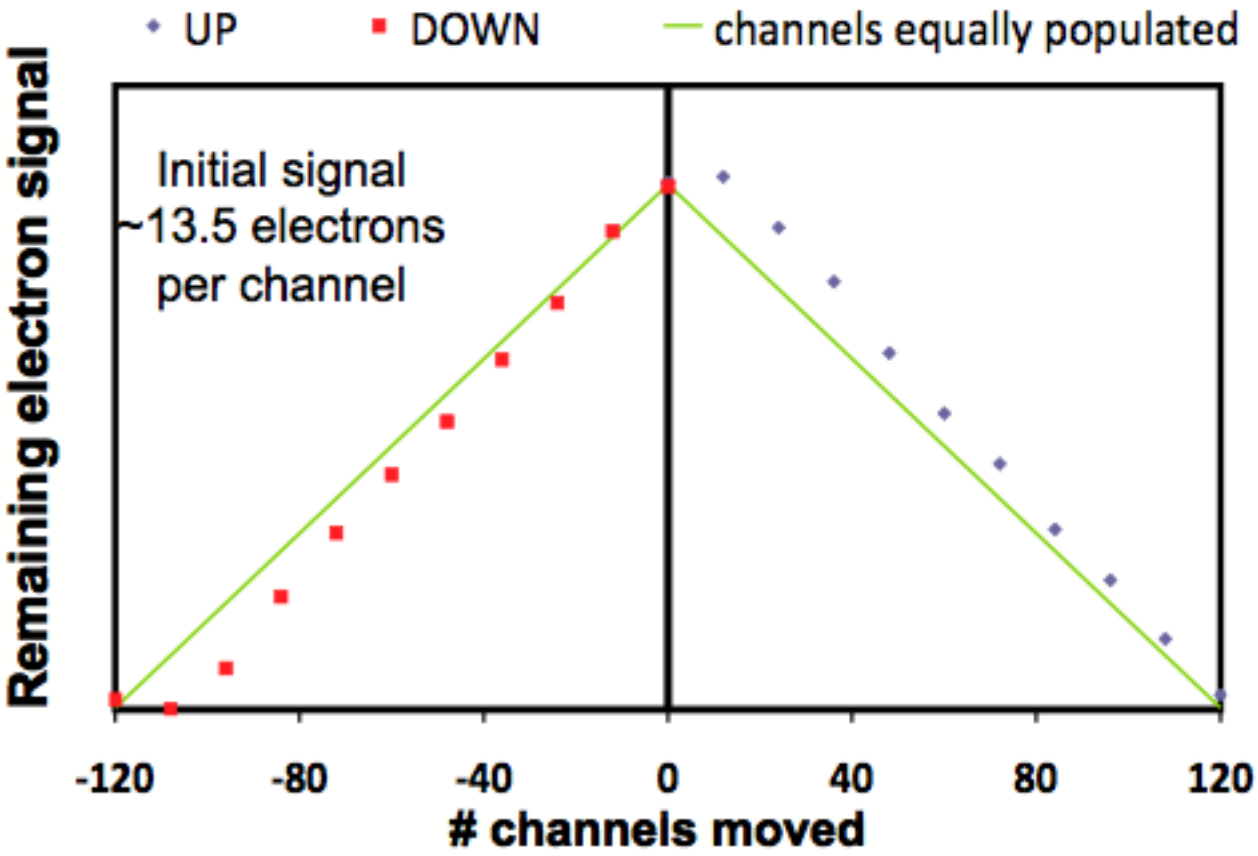
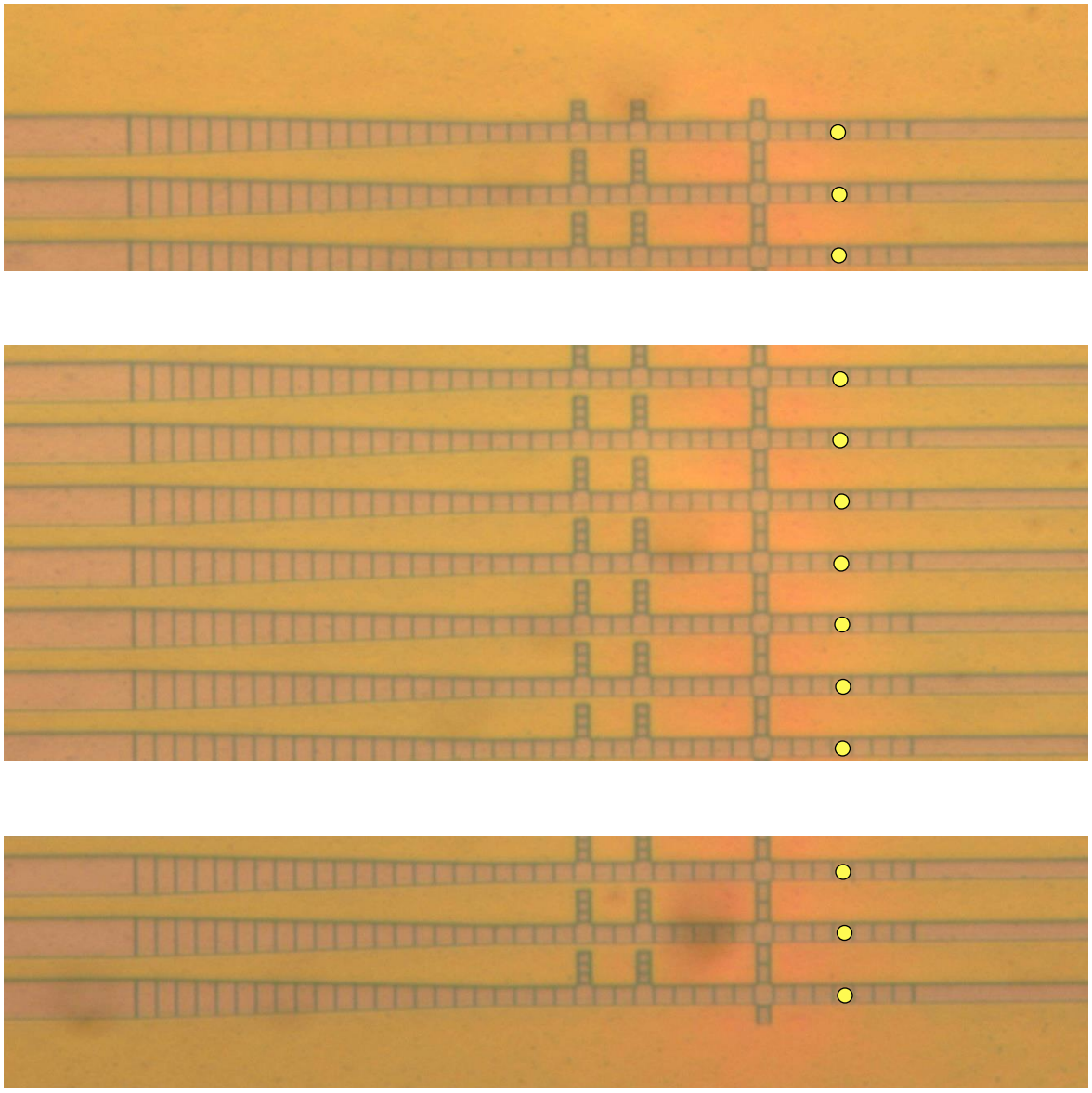


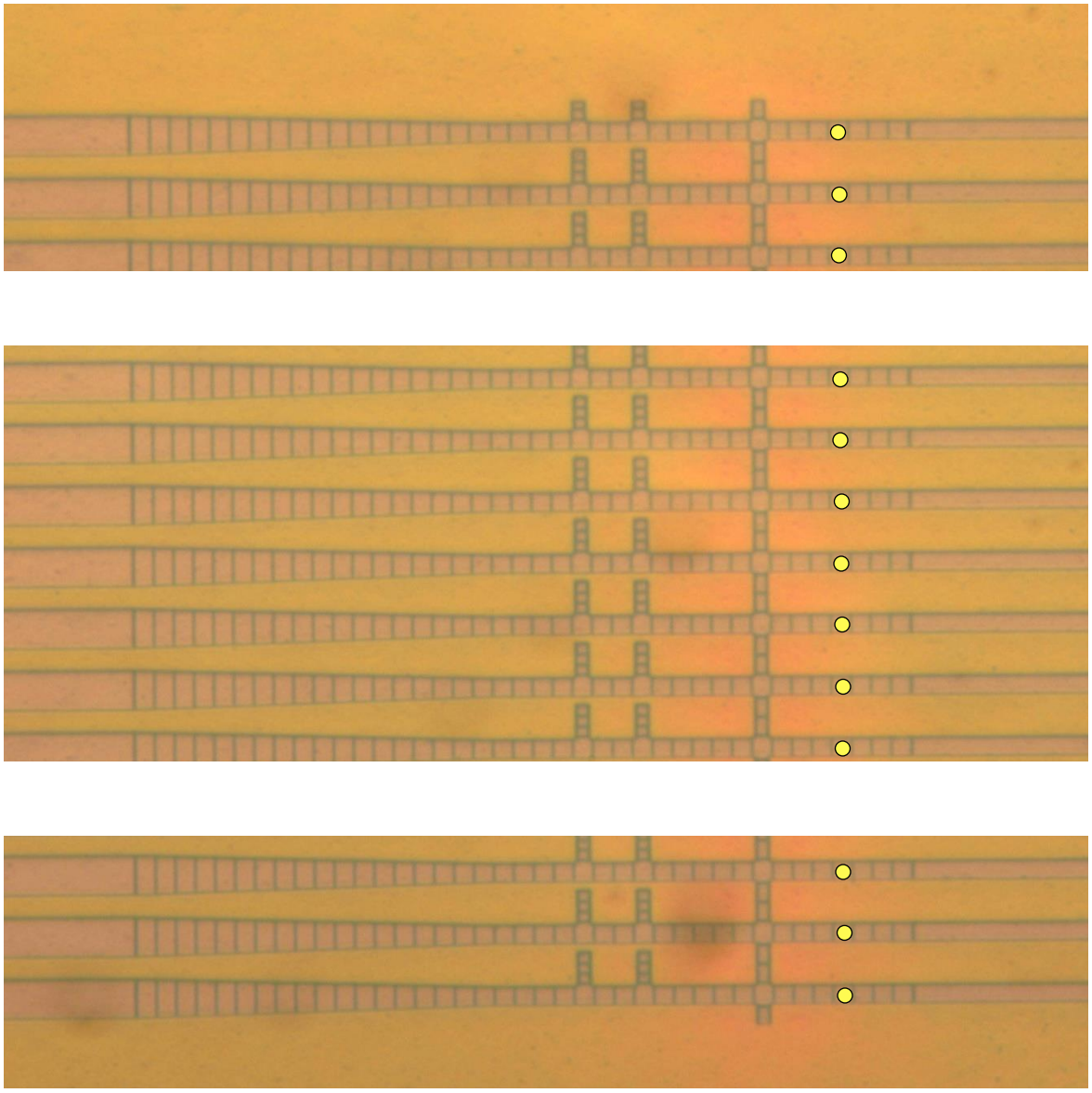
Channel Occupancy



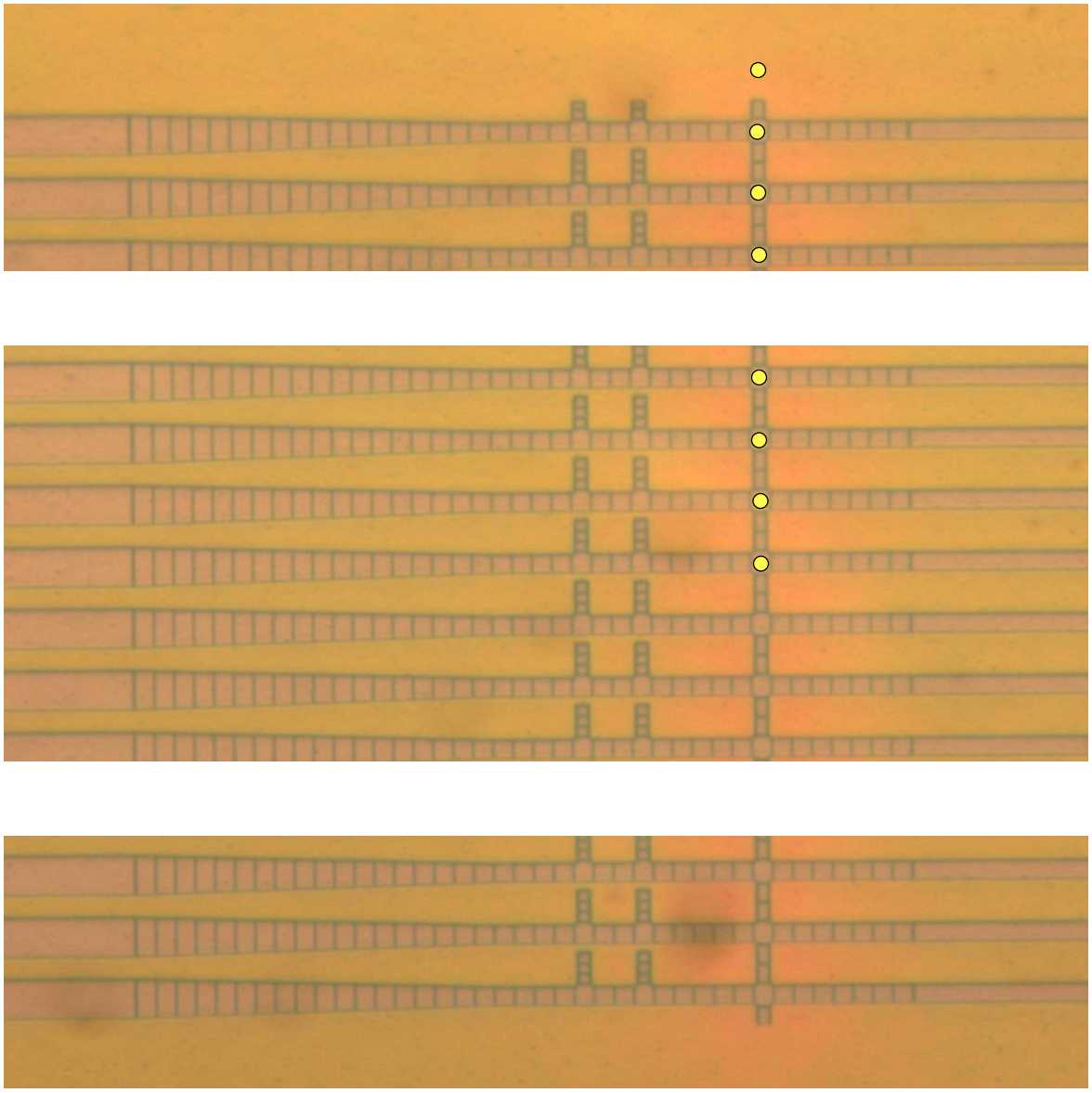
Vertical Clocking



Vertical Clocking

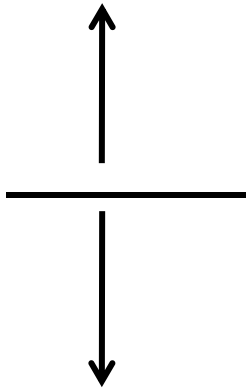


Vertical Clocking

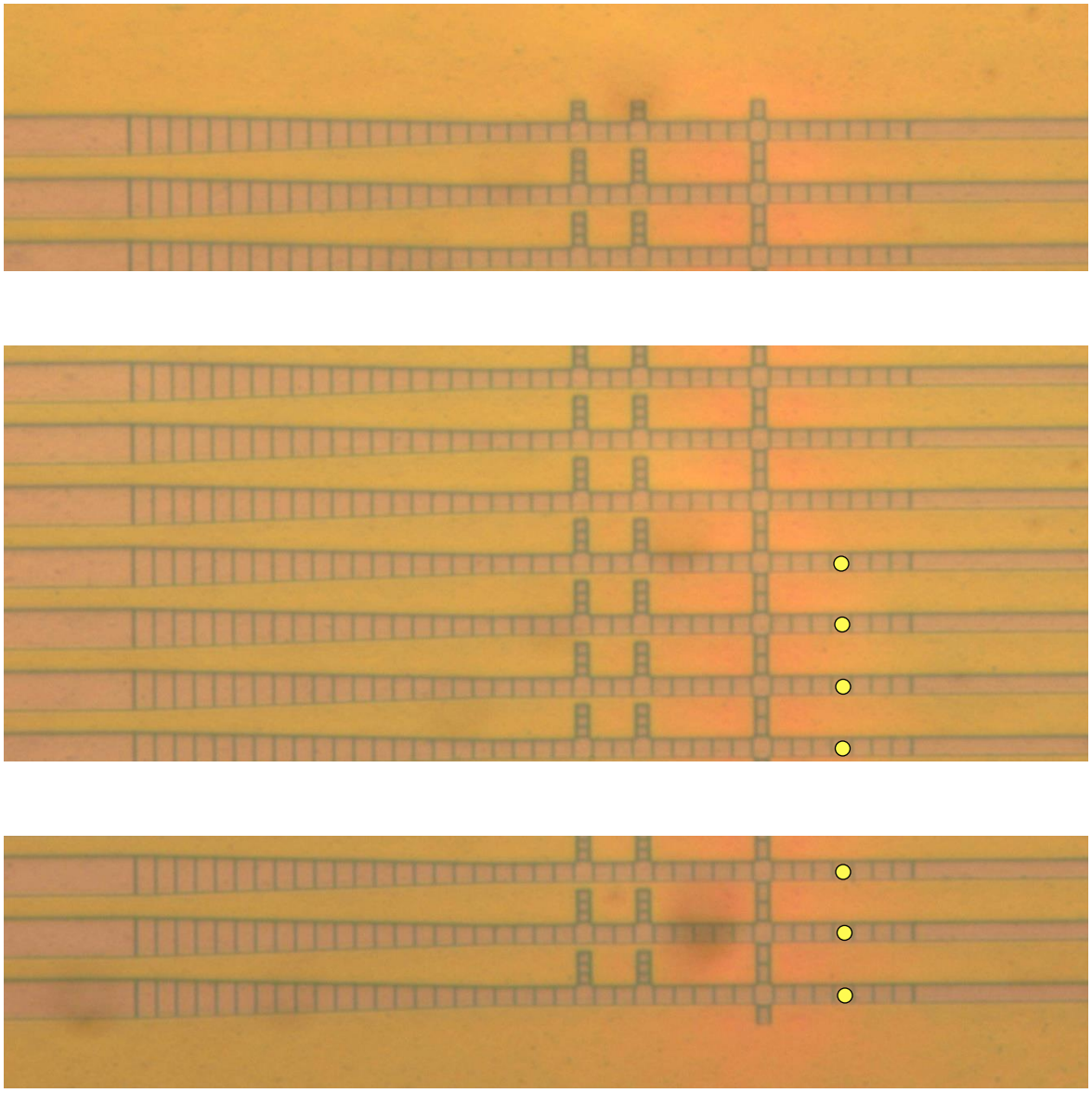


Vertical Clocking

60 Channels

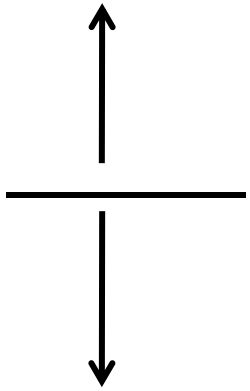


60 Channels

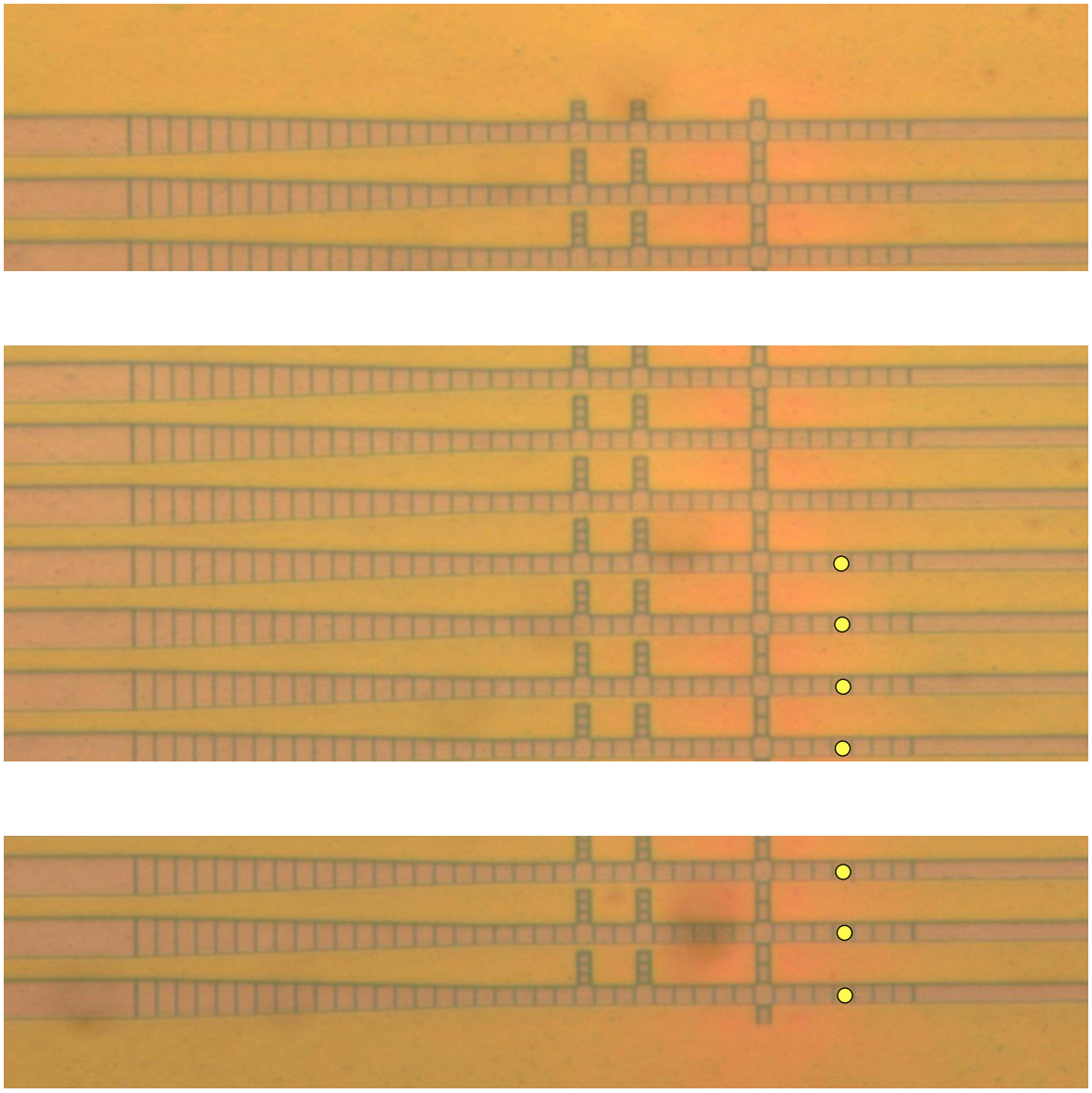


Vertical Clocking

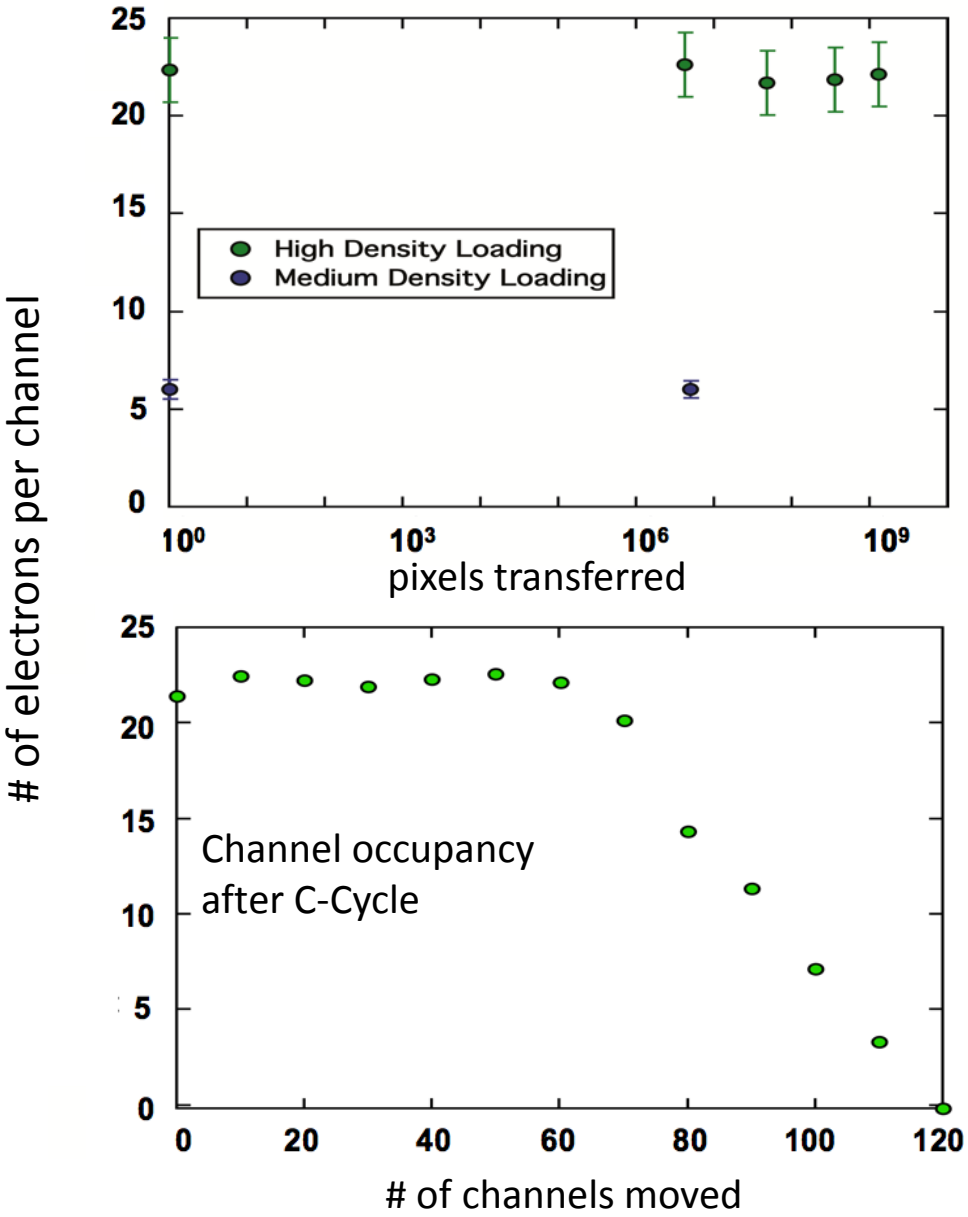
60 Channels



60 Channels



Vertical ("C-cycle") Efficiency



Conclusions for electrons on superfluid helium channels with silicon integrated circuits (Sandia device)

- Unprecedented reliability of a Charge Coupled Device
  - -Essentially a perfect Electron Transfer Efficiency

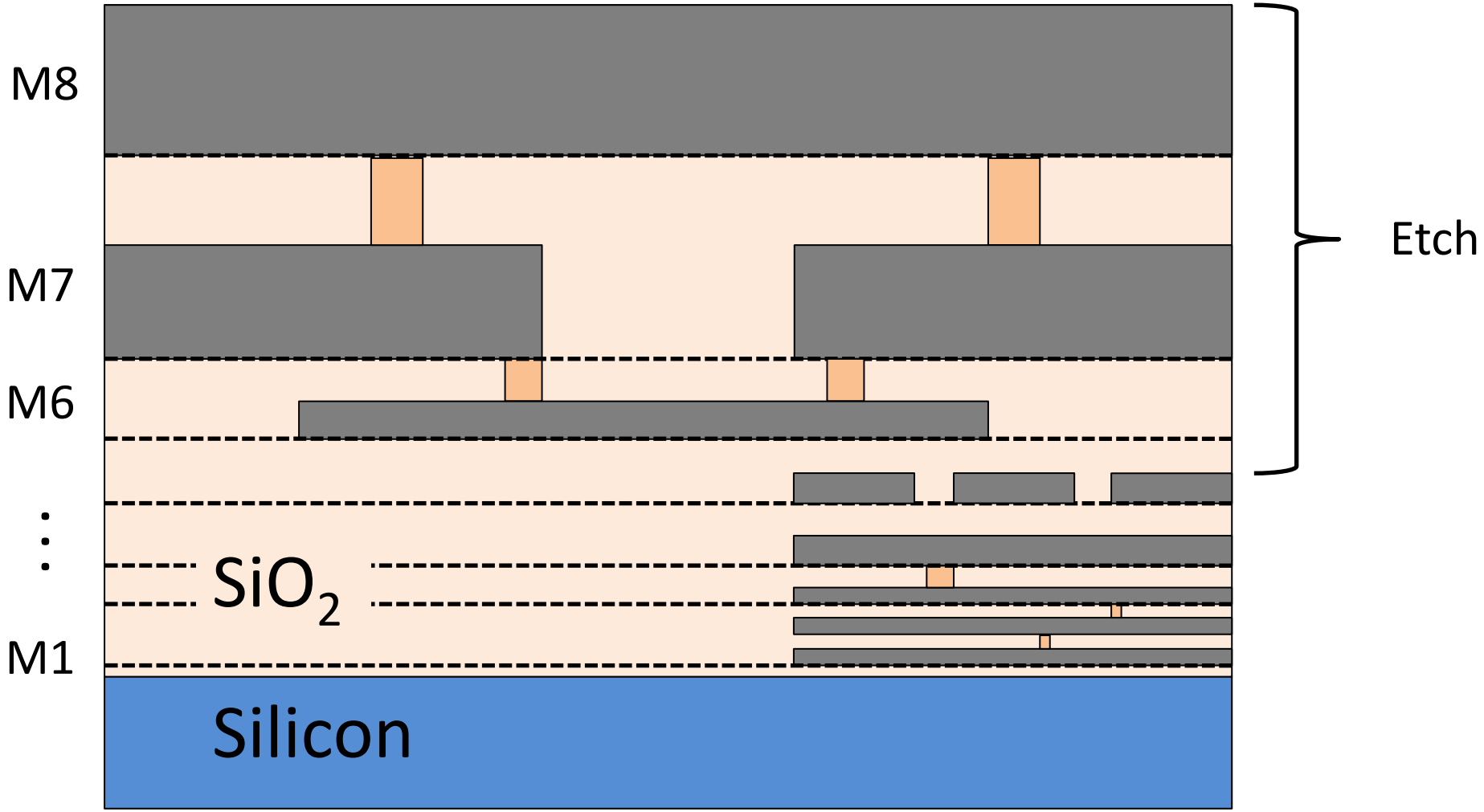
- 5 clock lines for full control
  - -2D Scalability: Move anywhere in our ~5000 position gate & channel array

- Si-Processing
  - -First, non-optimized design with standard silicon processing
  - -Possibilities for on-chip amplification
  - -On-chip multiplexer
  - -More…

Bradbury, Takita *et al.* PRL 107, 266803 (2011)

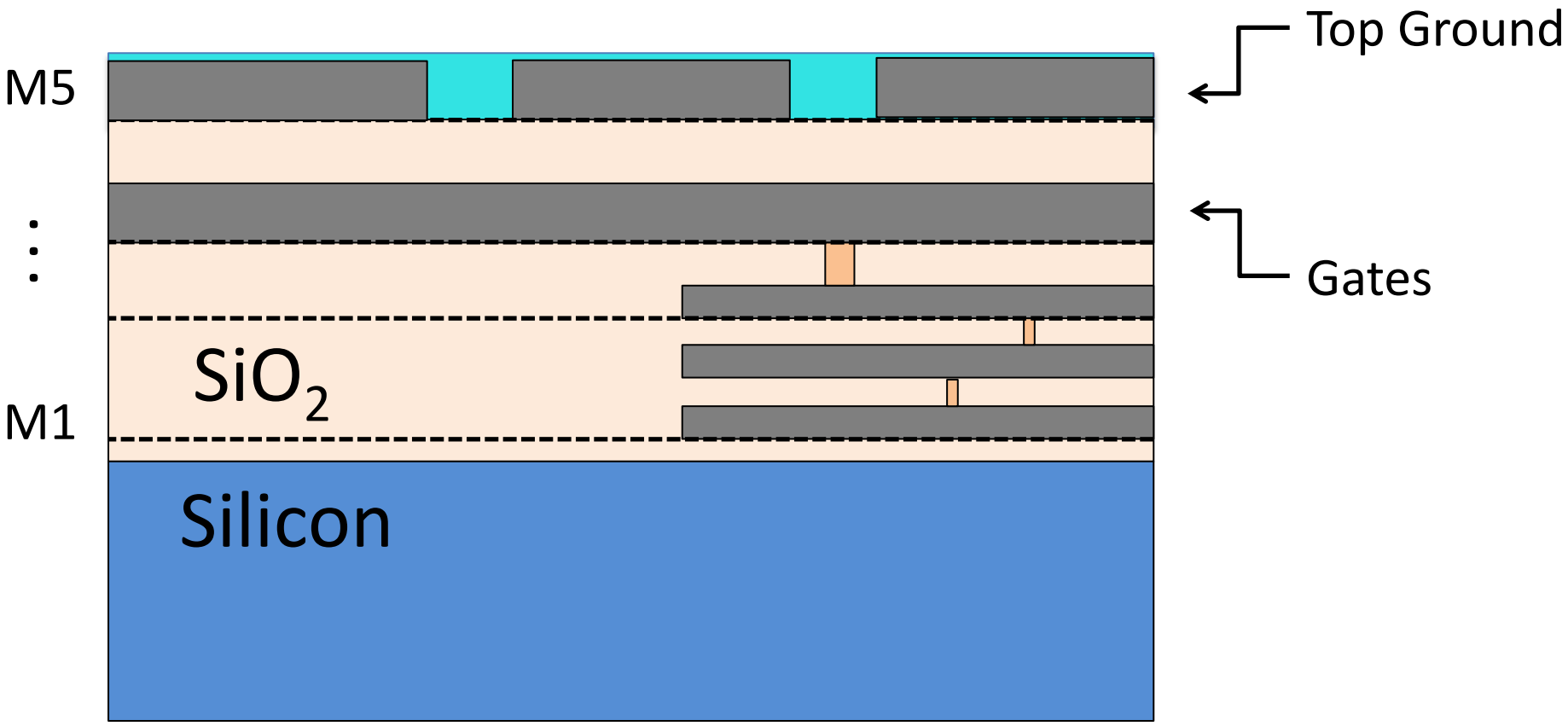
IBM CMOS

8 metal layers (Aluminum and Copper)

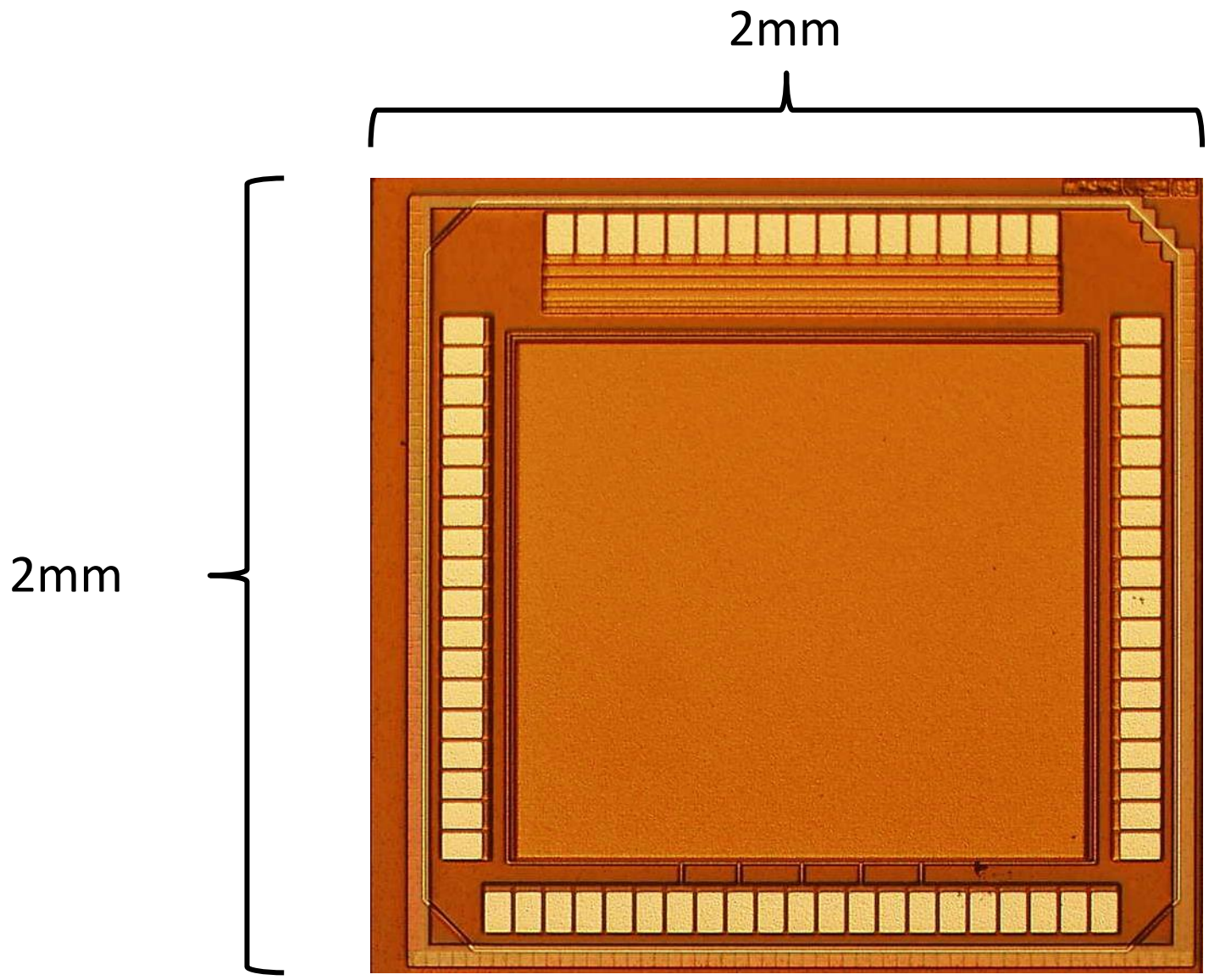


IBM CMOS

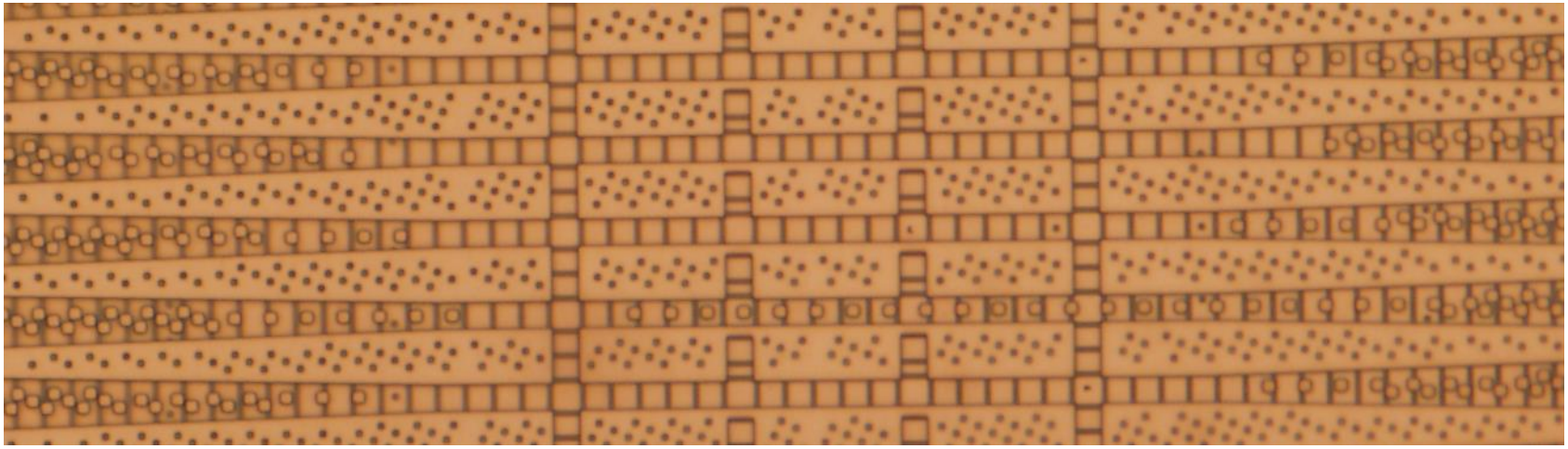
Channels using thin metals



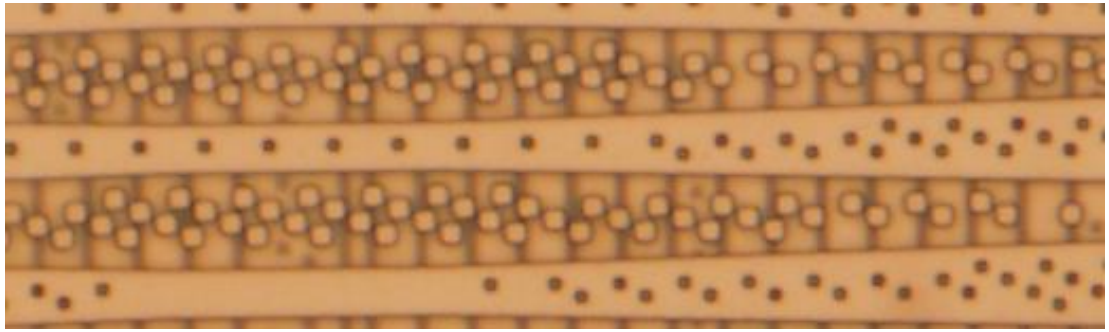
IBM CMOS

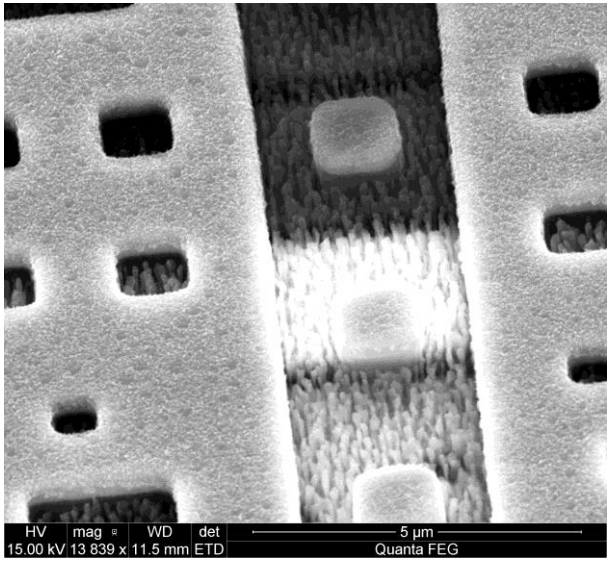


IBM CMOS



Filling and cheesing!!!!



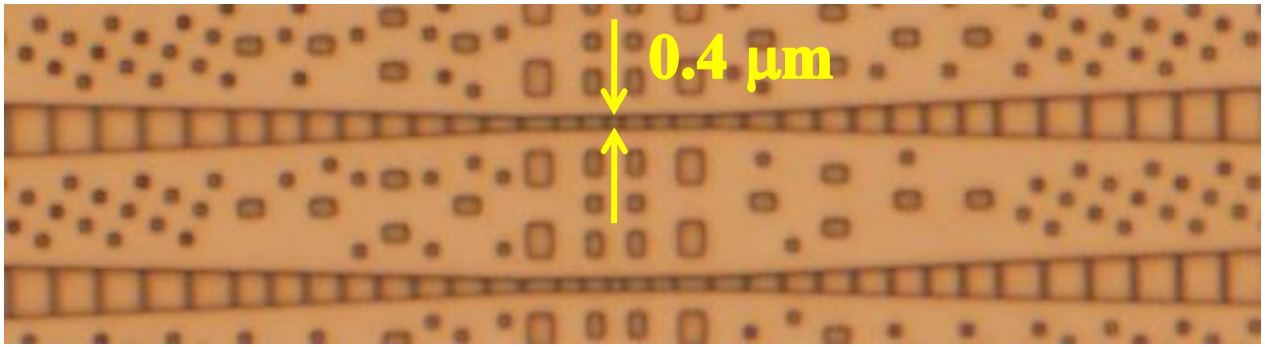


Electroplating? Electro chemistry?

IBM CMOS

Turnstile

Single Electron loading



ONE AT A TIME!!!

IBM CMOS

- Turnstile
- Quantum dots

Need better sensing

On-chip amplification?

What else?

IBM CMOS

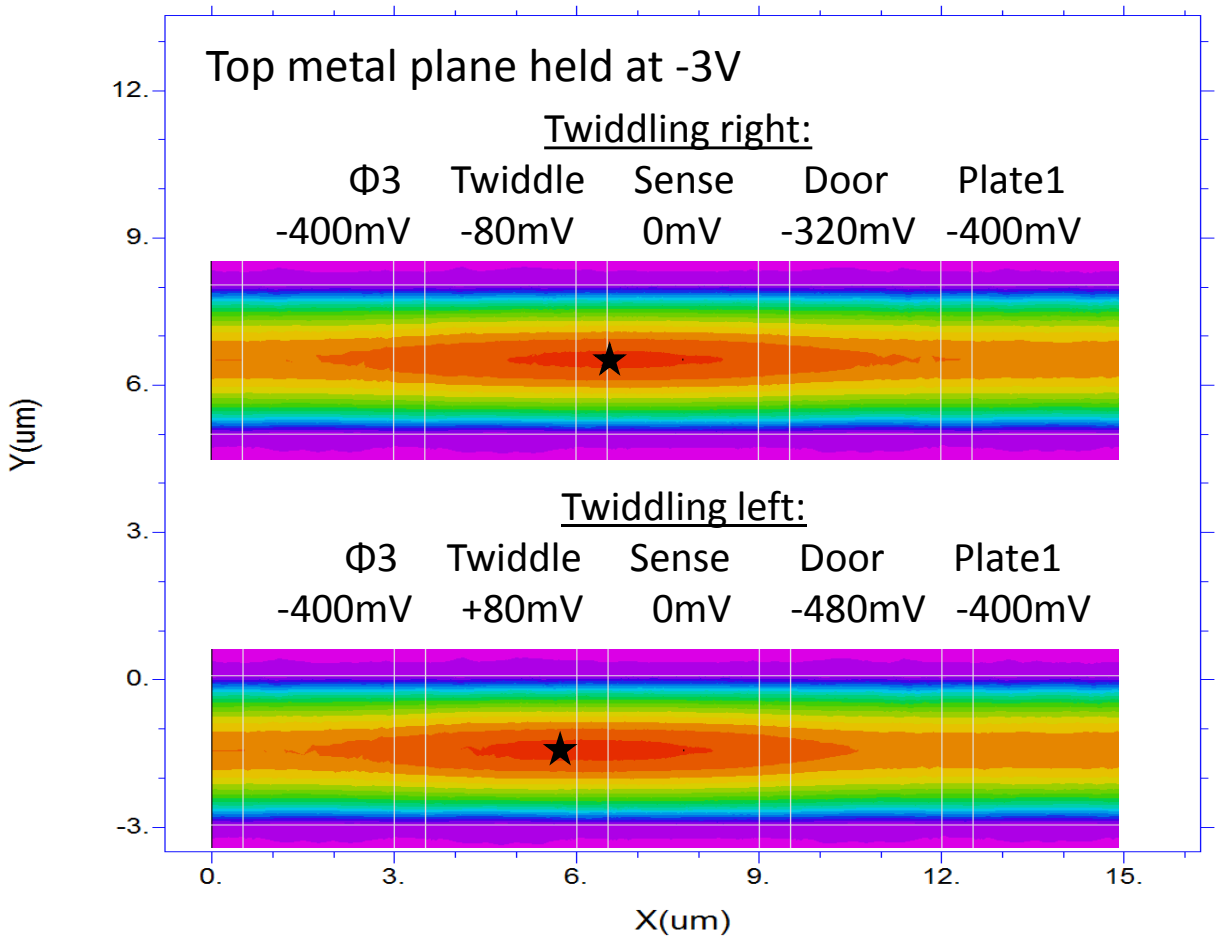
- Turnstile
- Quantum dots

Need better sensing

On-chip amplification?

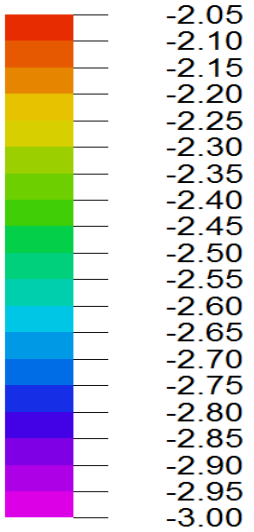
What else?

Twiddle Sensor: Potential Simulations



3 um channels

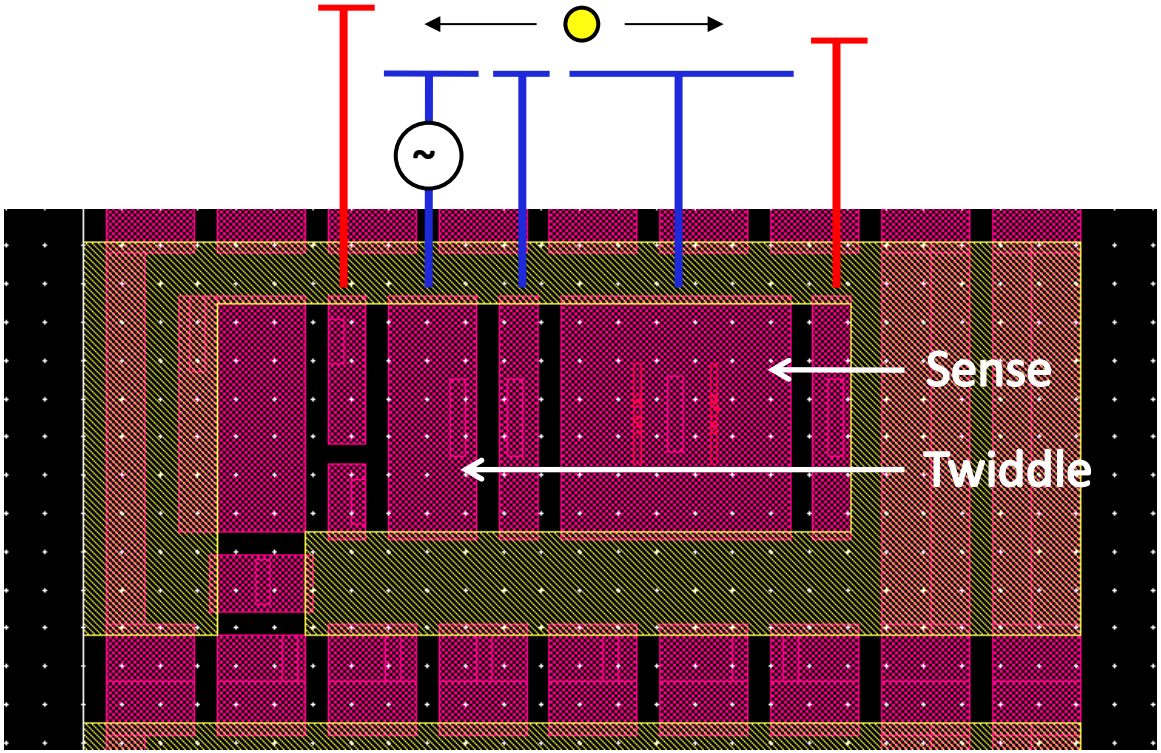
2.5 um wide gates

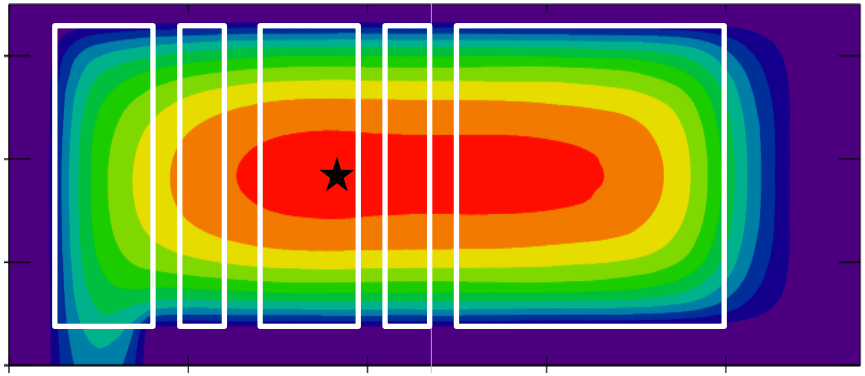


Electrical potential in volts at the helium surface above the channels

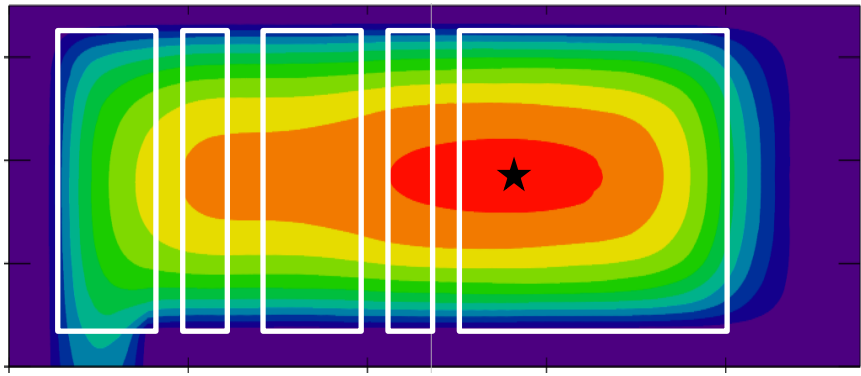
Wider gates!!!

- 6 X 6 um Sense gate
- Gate in between Sense and Twiddle

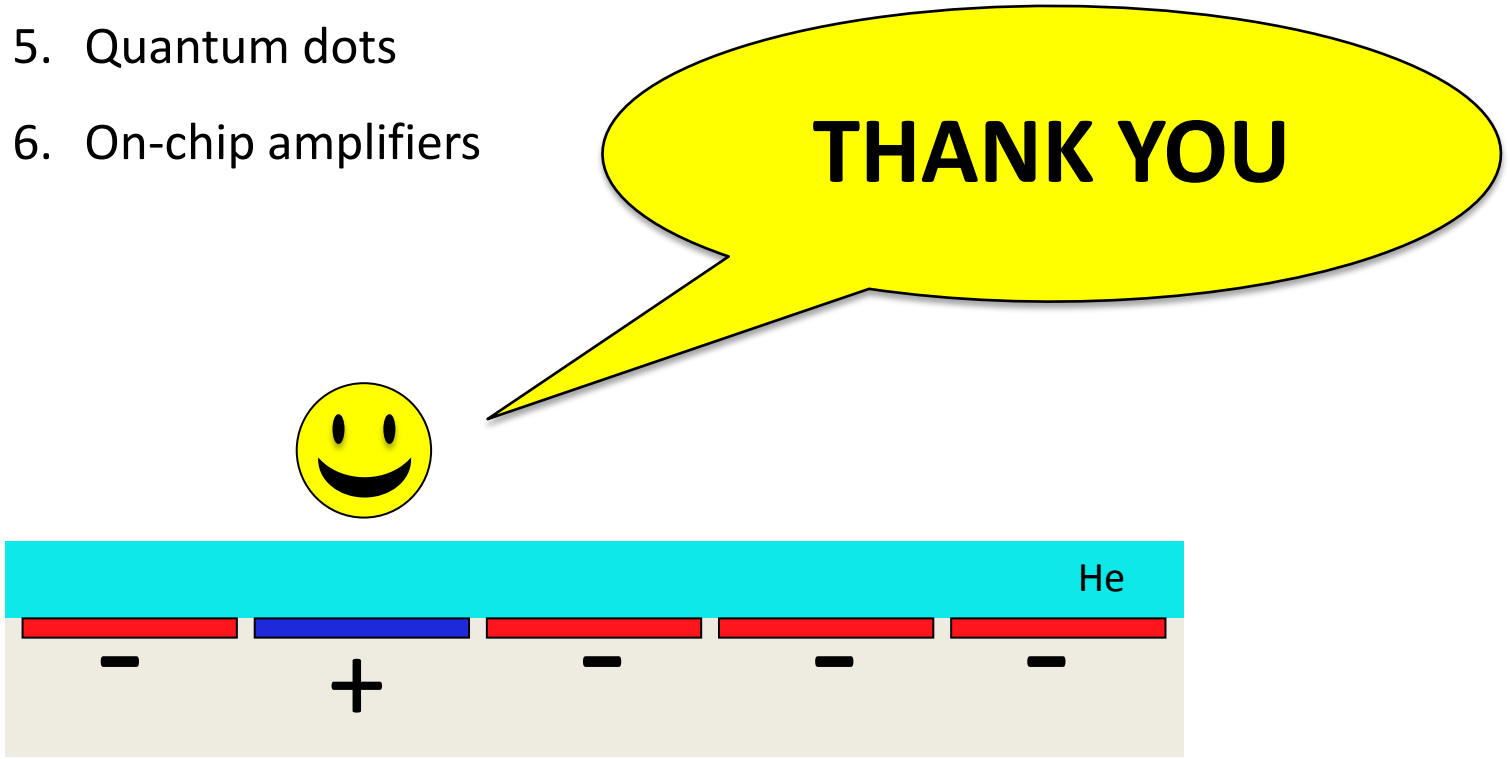




Twiddle



Sense

What do we do for our next chip???

1. Narrower channels (avoid filling)
2. Narrower gates (avoid cheesing)
3. Some wider gates (better sensing)
4. Turnstile
5. Quantum dots
6. On-chip amplifiers